

Compal Confidential

ICW50 Schematics Document

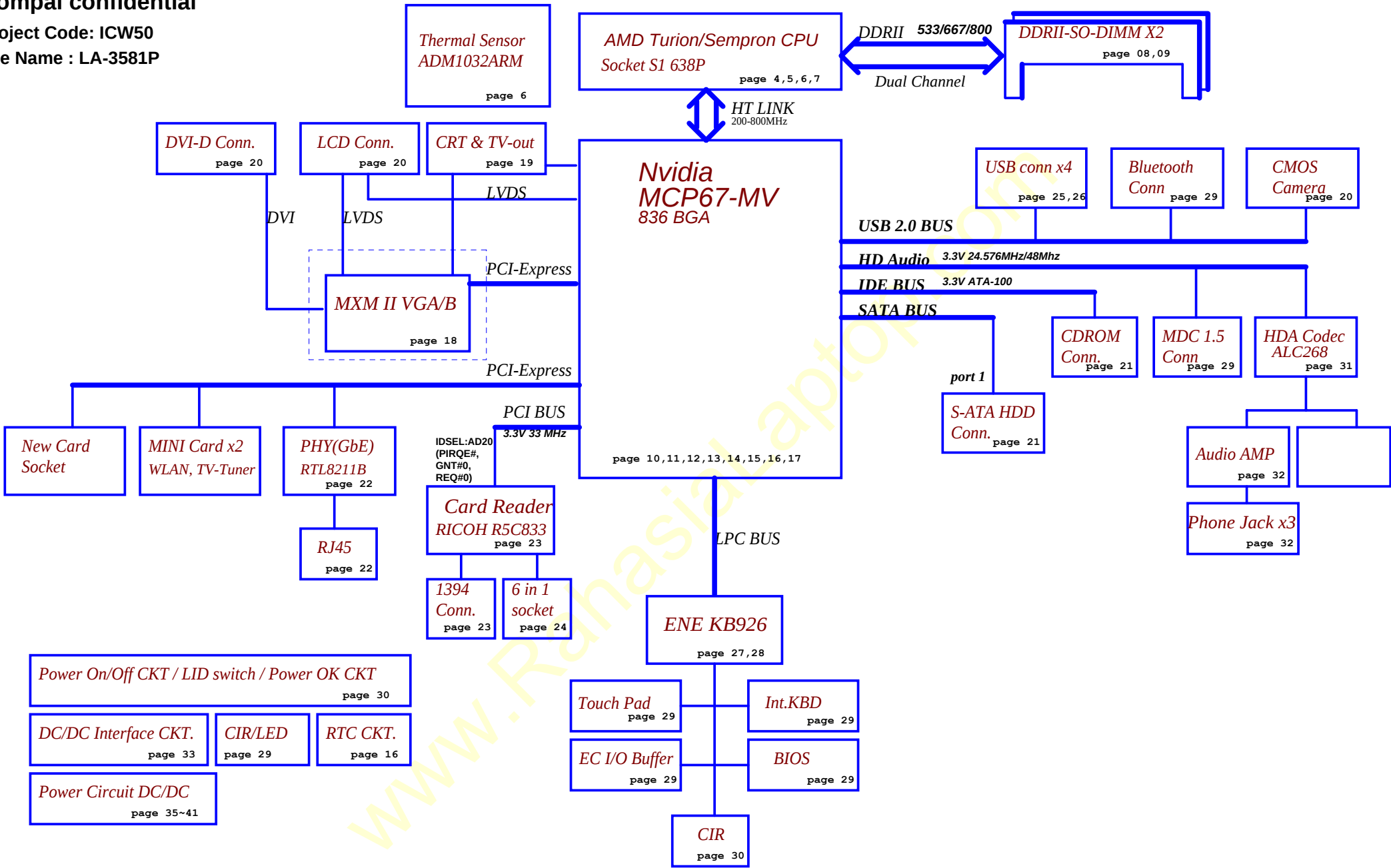
AMD Turion/Sempron + Nvidia MCP67-MV

2007 / 04 / 20 Rev:1.0 FOR Pre-MP

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Cover Sheet
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				Date: Friday, April 20, 2007	Rev 1.0
				Sheet 1 of 42	

Compal confidential

Project Code: ICW50
File Name : LA-3581P



Security Classification		Compal Secret Data		Title	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	BLOCK DIAGRAM	
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				Date:	Friday, April 20, 2007
				Sheet	2 of 42
				Rev	1.0

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON*
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW/+3V/+3VAUX	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD20	0	PIRQE

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	UMA (0V)
1	DISCRETE (3.3V)
2	
3	
4	
5	
6	
7	

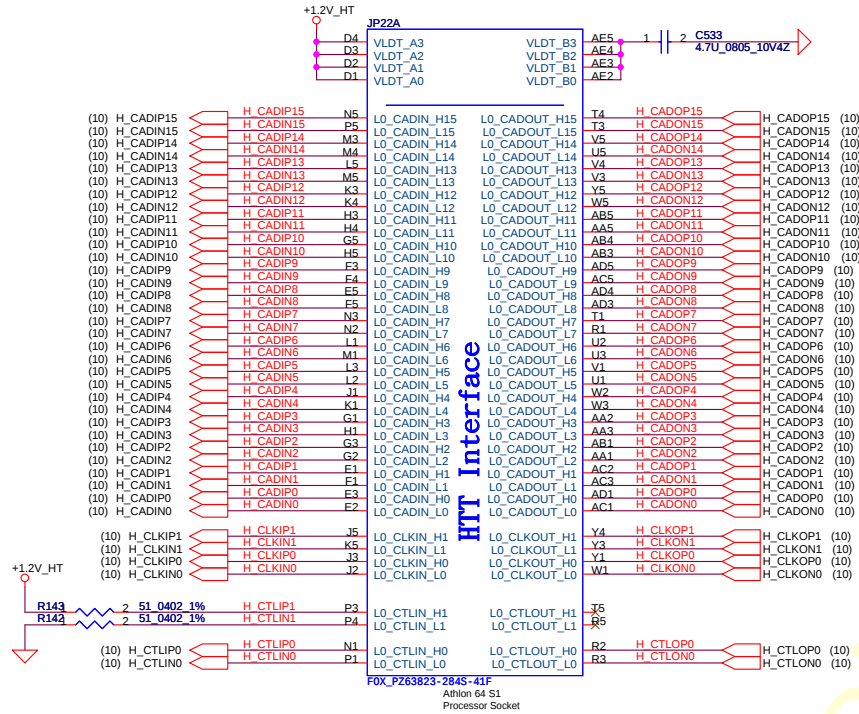
SKU ID	SKU
0	B - PHASE
1	C - PHASE
2	
3	
4	
5	
6	
7	

[illegible]

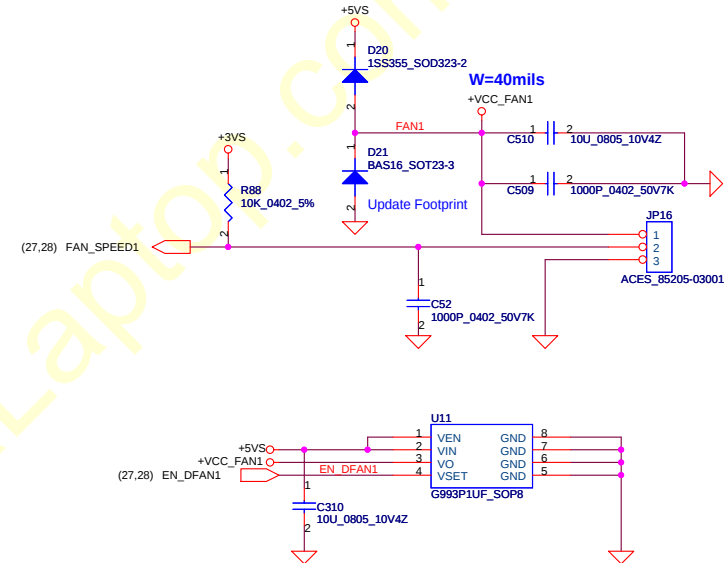
Security Classification	Compal Secret Data			Title TABLE OF CONTENTS Size Document Number ICW50 / ICY70 LA-3581P Rev 1.0		
Issued Date	2006/08/18	Deciphered Date	2007/8/18			
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PROCESSOR HYPERTRANSPORT INTERFACE

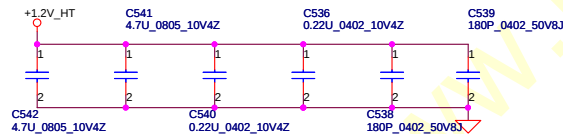
VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



FAN Conn



FAN1 Conn



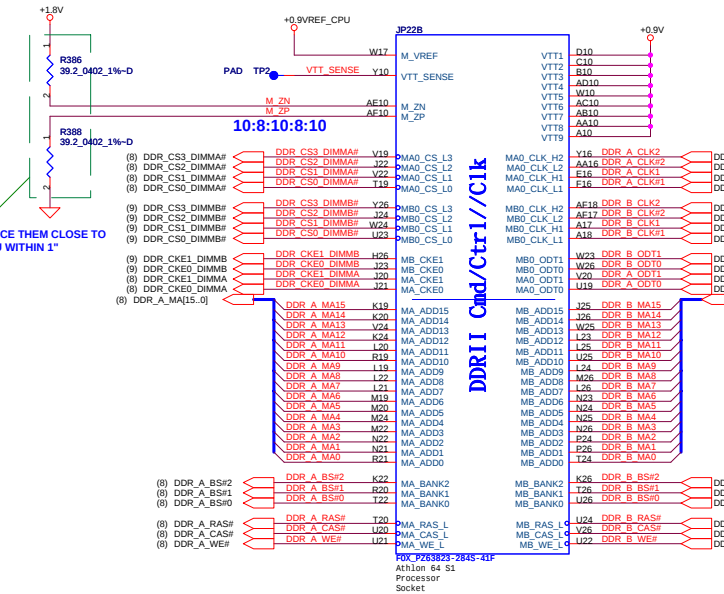
LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS PLACE CLOSE TO VLDTO POWER PINS

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	AMD CPU HT I/F	
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				Date: Friday, April 20, 2007	Sheet 4 of 42

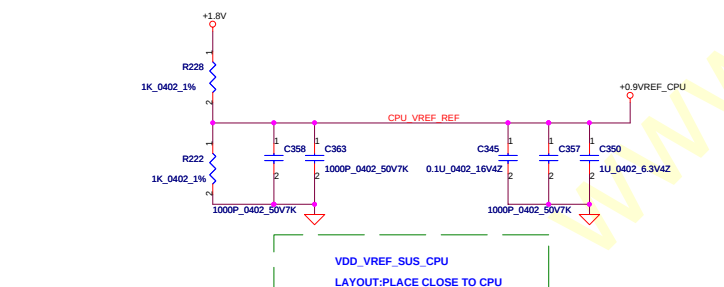
Processor DDR2 Memory Interface

VDD VTT SUS_CPU IS CONNECTED TO THE VDD VTT SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

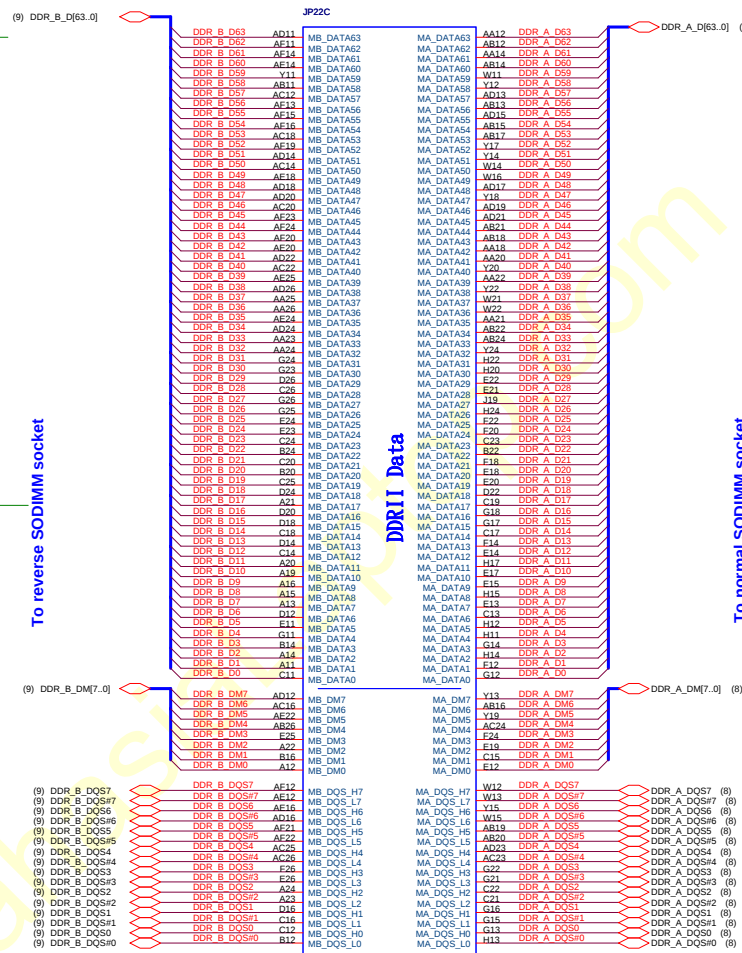


PLACE THEM CLOSE TO CPU WITHIN 1"

PLACE CLOSE TO PROCESSOR WITHIN 1.2 INCH

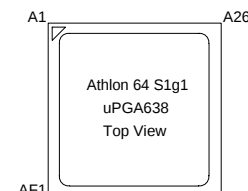


VDD_VREF_SUS_CPU LAYOUT: PLACE CLOSE TO CPU



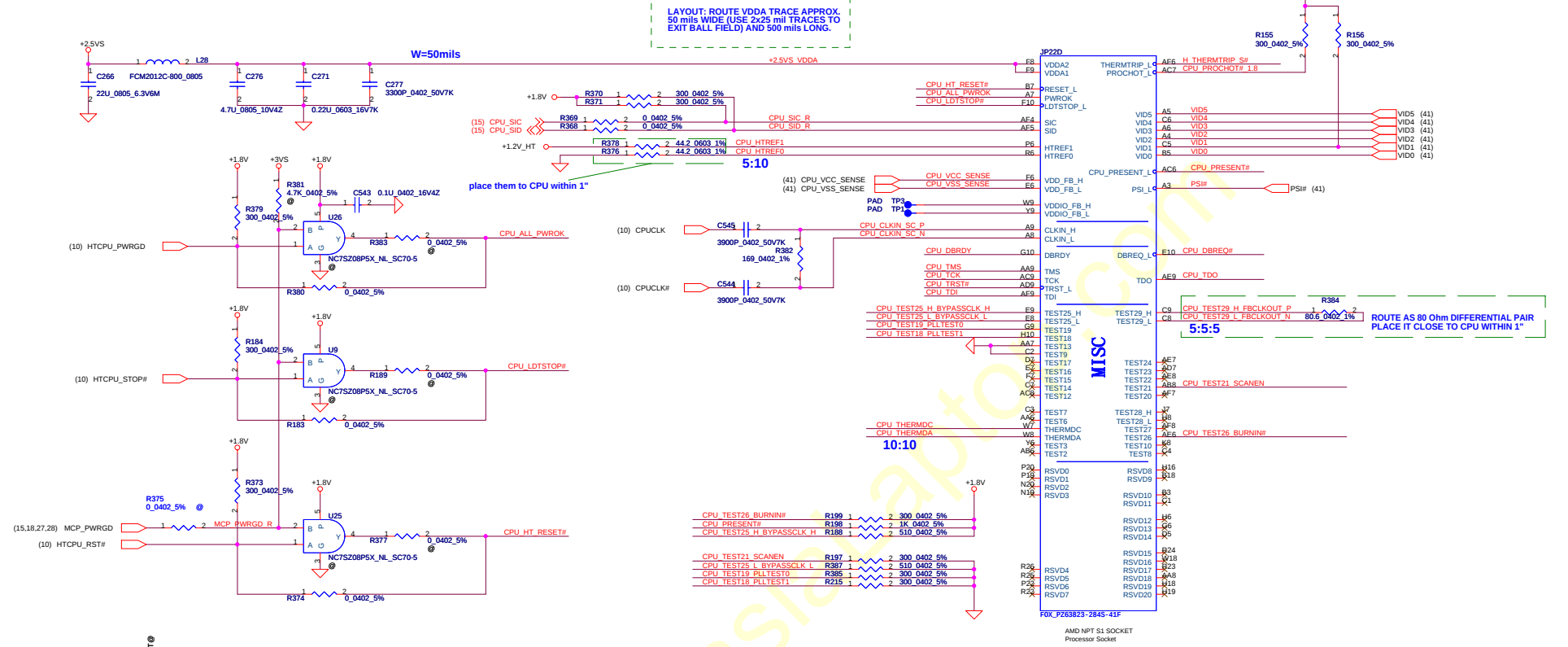
To reverse SODIMM socket

To normal SODIMM socket

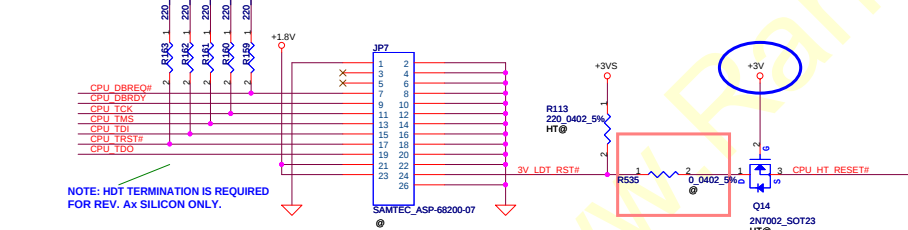


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Document Number: ICW50 / ICY70 LA-3581P				Date: Friday, April 20, 2007	Sheet: 5 of 42

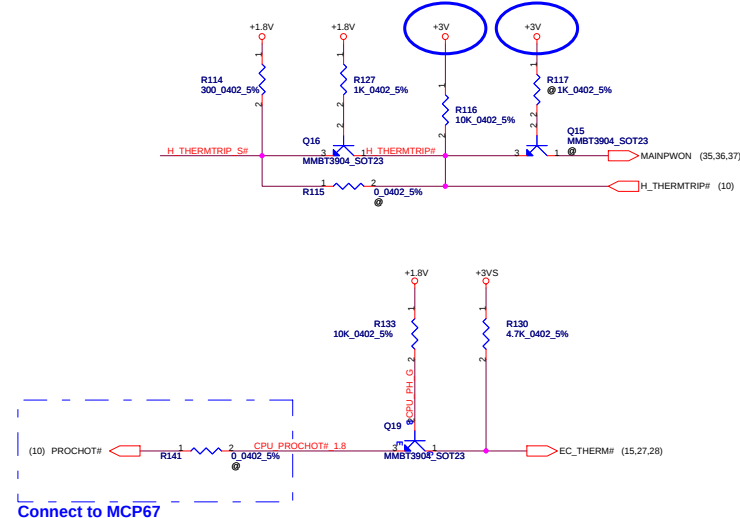
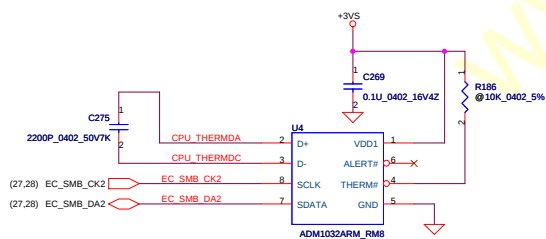
ATHLON Control and Debug



HDT Connector

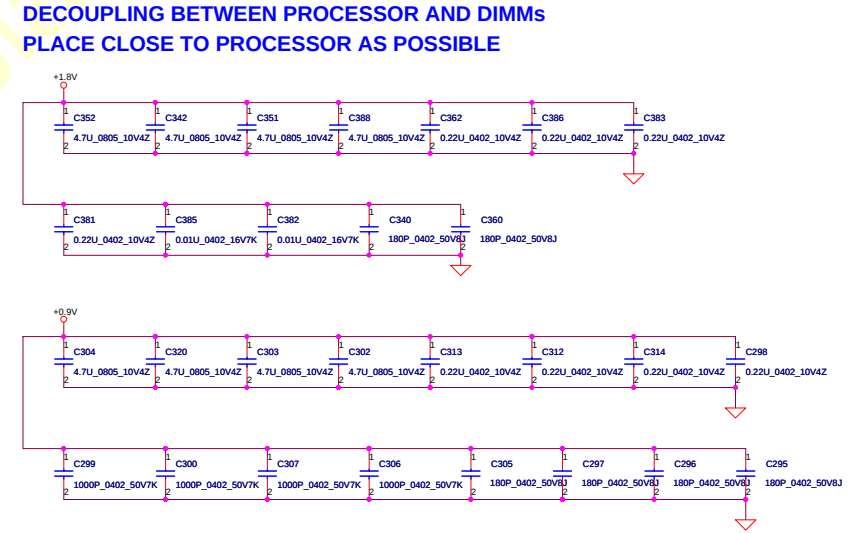
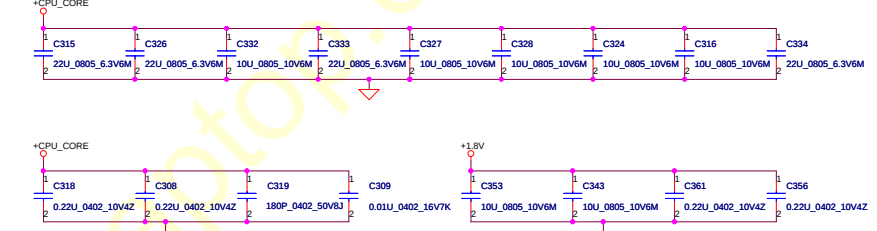
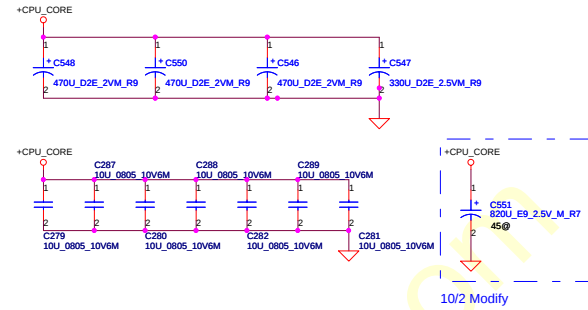
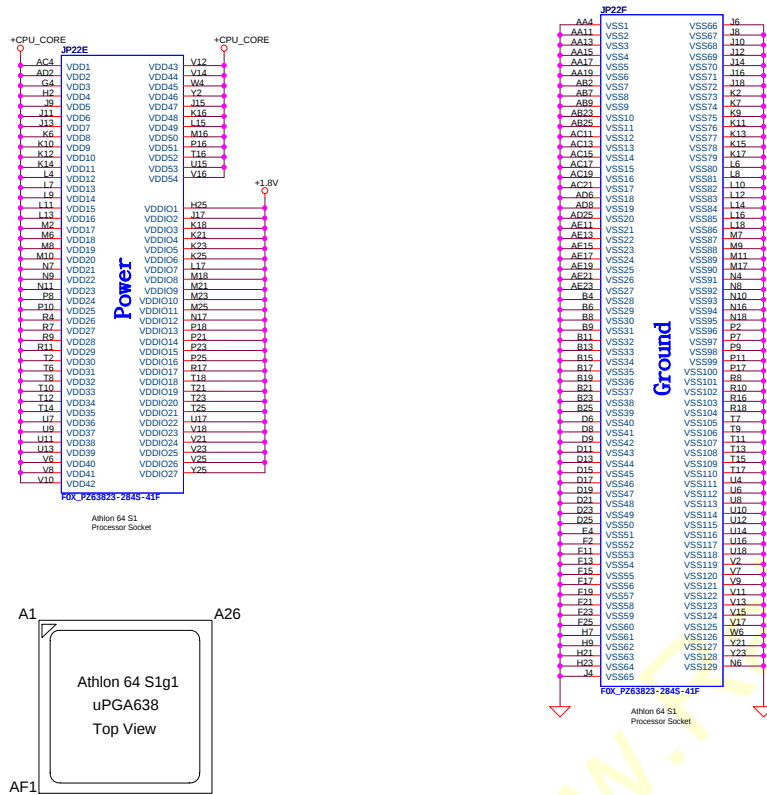


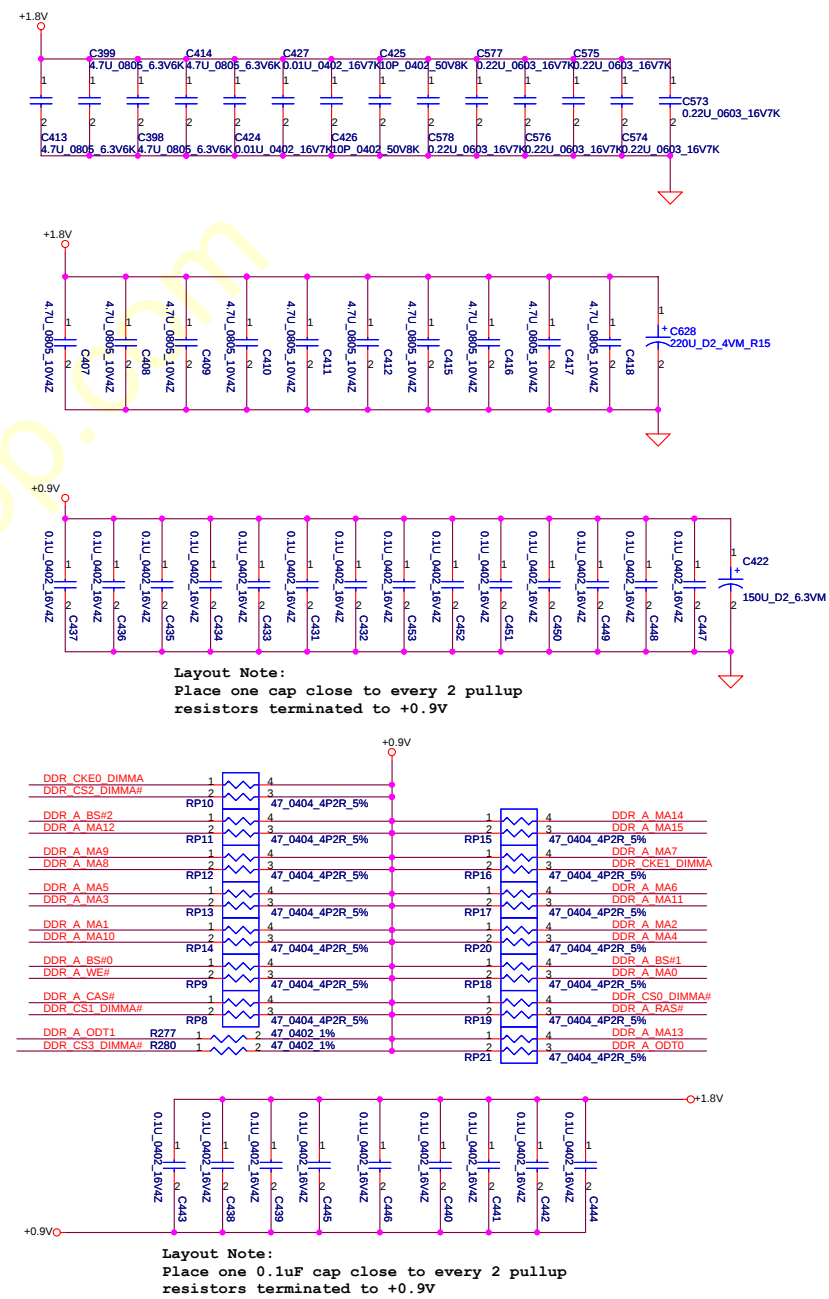
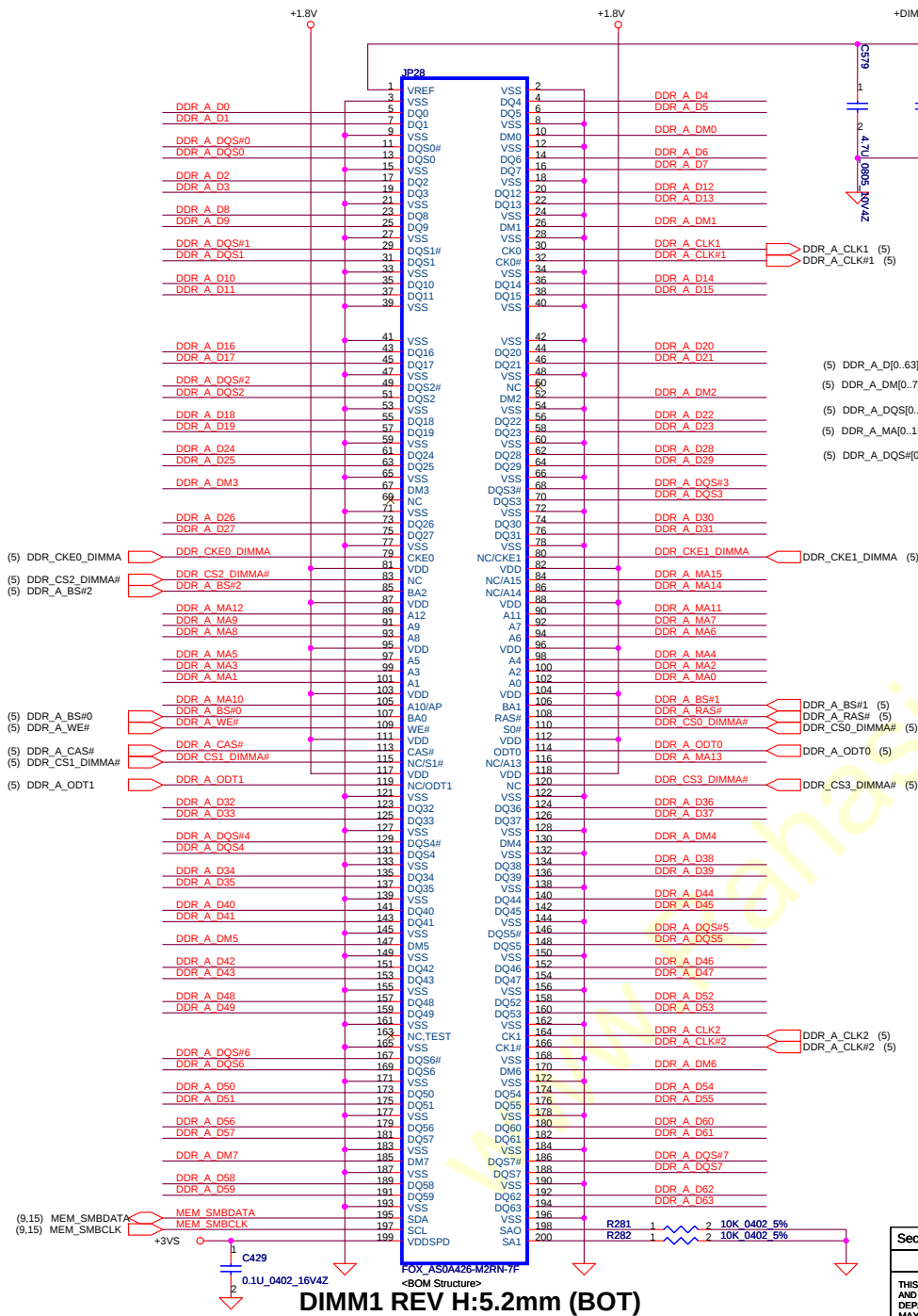
PVT Modify 2007/03/22

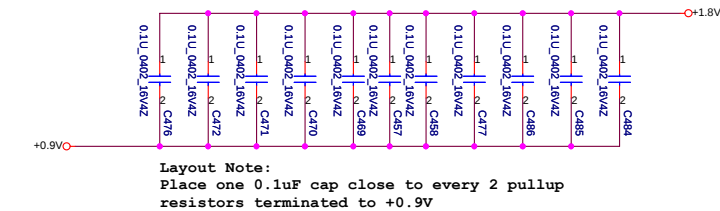
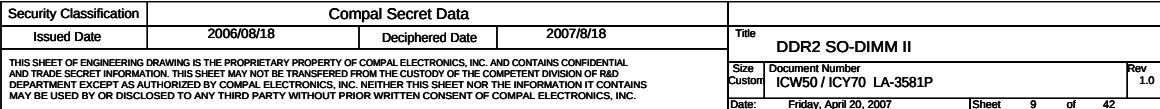


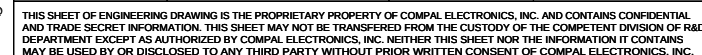
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				C	ICW50 / ICY70 LA-3581P
				Date:	Friday, April 20, 2007
				Sheet	6 of 42
				Rev	1.0

PROCESSOR POWER AND GROUND



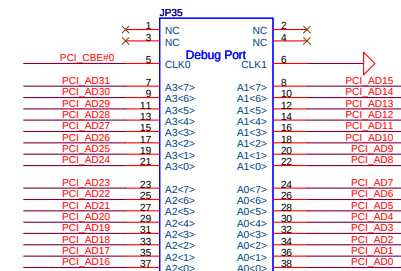
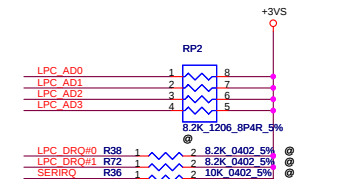
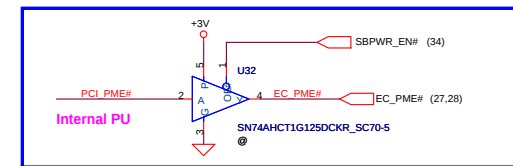








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						Custom		ICW50 / ICY70 LA-3581P		1.0			
						Date:		Friday, April 20, 2007		Sheet		12 of 42	



Security Classification		Compal Secret Data		Title MCP67 PCI/ LPC/ IDE				
Issued Date	2006/08/18	Deciphered Date	2007/8/18					
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						Custody	ICW50 / ICY70 LA-3581P	
Date:		Friday, April 20, 2007		Sheet	13 of 42			

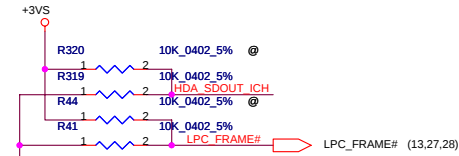
(21)	SATA_STX_C_DRX_P0	SATA STX C DRX P0	0.01U 040Z 16V7K	1	2	C512	SATA_STX_DRX_P0	AE4	SATA_A0_TX_P
(21)	SATA_STX_C_DRX_N0	SATA STX C DRX N0	0.01U 040Z 16V7K	1	2	C511	SATA_STX_DRX_N0	AE5	SATA_A0_TX_N
(21)	SATA_DTX_C_SRX_N0	SATA DTX C SRX N0						AG5	SATA_A0_RX_N
(21)	SATA_DTX_C_SRX_P0	SATA DTX C SRX P0						AG6	SATA_A0_RX_P

(21) SATA_STX_C_DRX_P1  SATA_STX_C_DRX_P1 0.01U 0402 16V7K 1 2 C514 SATA_STX_DRX_P1 AG4 SATA_B0_TX_P

(21) SATA_STX_C_DRX_N1  SATA_STX_C_DRX_N1 0.01U 0402 16V7K 1 2 C513 SATA_STX_DRX_N1 AG3 SATA_B0_TX_N

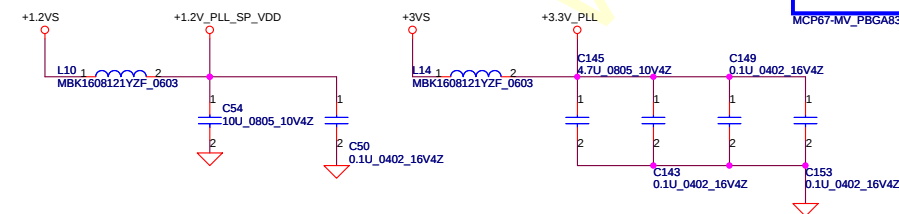
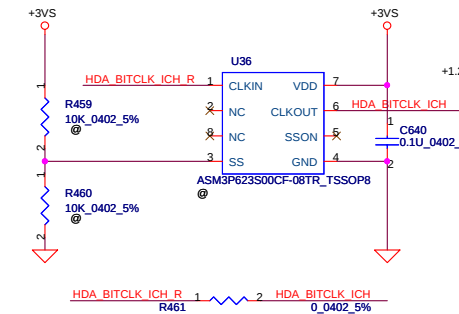
(21) SATA_DTX_C_SRX_N1  SATA_DTX_C_SRX_N1 SATA2@ AH3 SATA_B0_RX_N

(21) SATA_DTX_C_SRX_P1  SATA_DTX_C_SRX_P1 AH2 SATA_B0_RX_P



***DEFAULT**

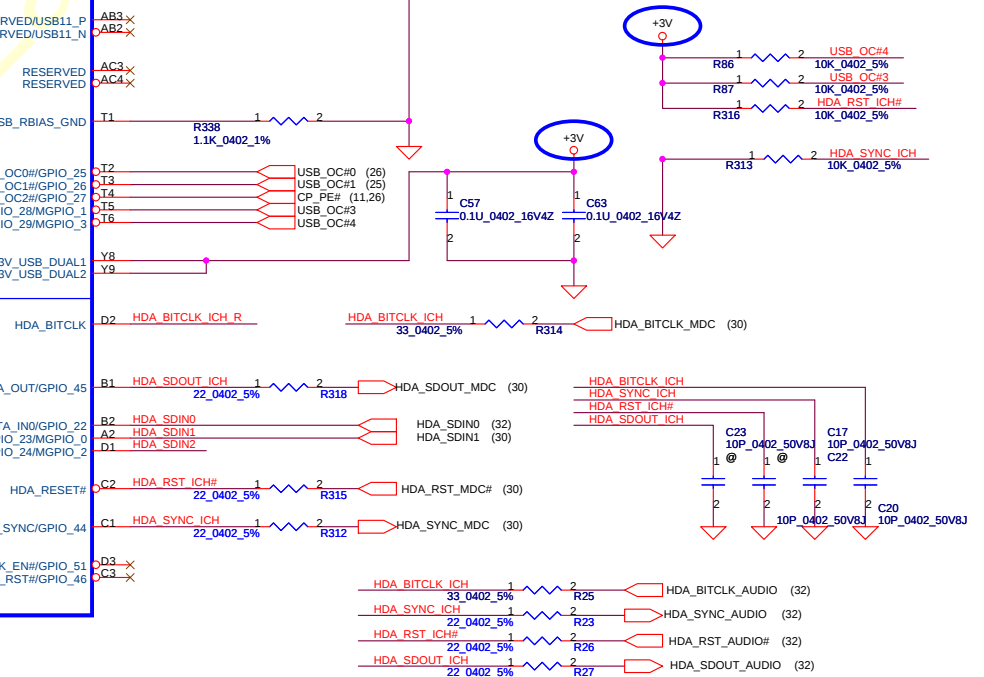
Schematic diagram of the temperature sensor circuit. The circuit includes a 5V supply, a red LED (SATA_LED#), a resistor R108, and a microcontroller. The LED's anode is connected to the 5V supply, and its cathode is connected to a node labeled '1'. This node is connected to a 2.49K resistor (R108) which is connected to a node labeled '2'. Node '2' is connected to the A14 pin of the microcontroller, which is labeled 'SATA_TERM'. The microcontroller's D4 pin is connected to the SATA_LED# signal line, which is also labeled 'SATA_LED#/GPIO'. The signal line is connected to the (27,28) pins of the microcontroller.



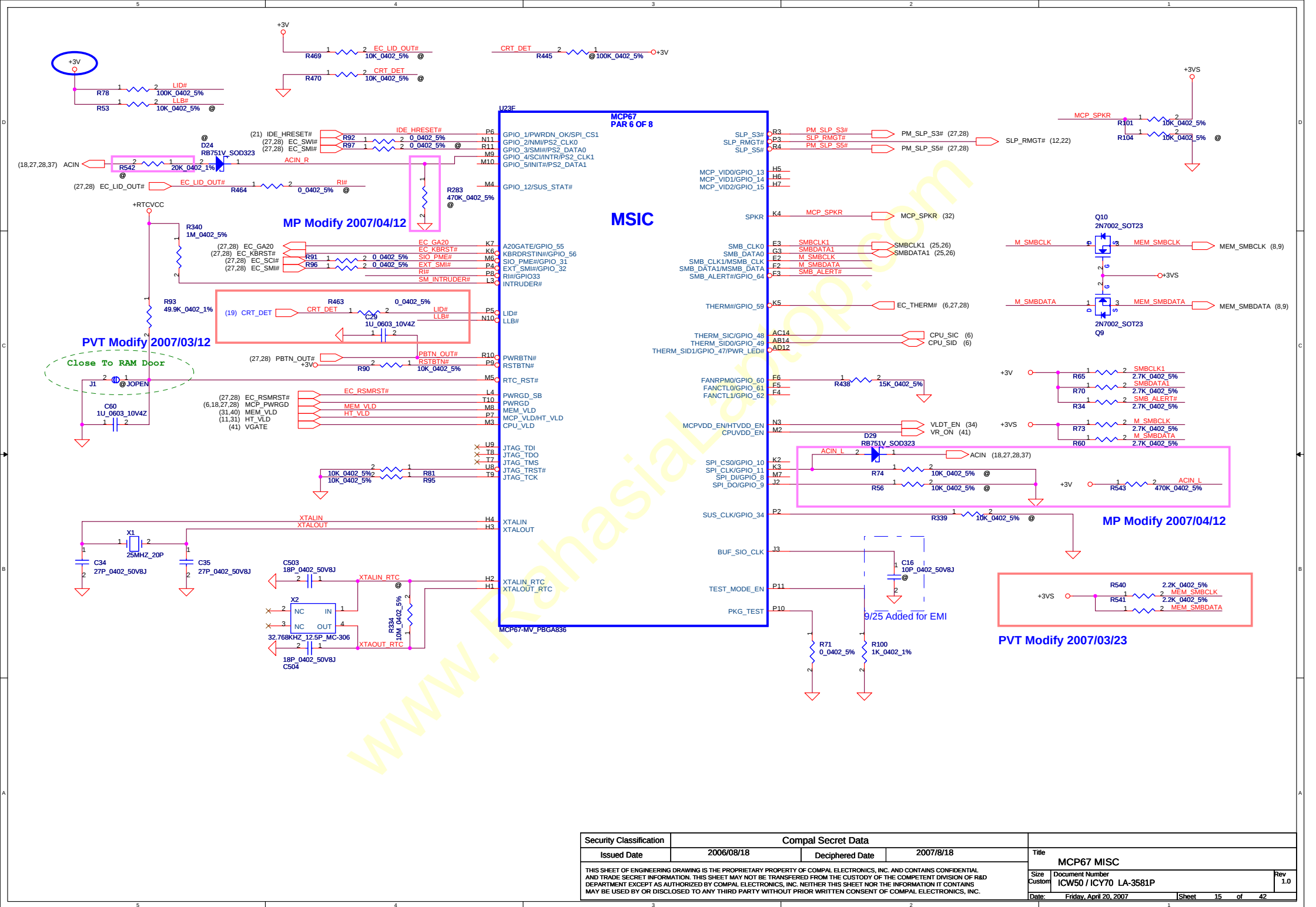
USB

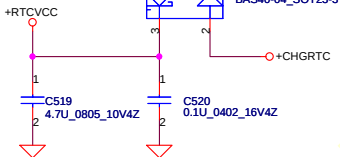
Pin	Label	Component	Value	Pin	Label	Component	Value	Pin	Label	Component	Value
USB0_P	U3	USB20_P0			USB20_P0	(26)			USB PORT_1		
USB0_N	U2	USB20_N0			USB20_N0	(26)					
		R343	15K_0402_5%		R346	15K_0402_5%					
USB1_P	U4	USB20_P1			USB20_P1	(26)			USB PORT_1		
USB1_N	U5	USB20_N1			USB20_N1	(26)					
		R342	15K_0402_5%		R341	15K_0402_5%					
USB2_P	U6	USB20_P2			USB20_P2	(25)			USB/B Connector		
USB2_N	U7	USB20_N2			USB20_N2	(25)					
		R84	15K_0402_5%		R80	15K_0402_5%					
USB3_P	V3	USB20_P3			USB20_P3	(25)			USB/B Connector		
USB3_N	V2	USB20_N3			USB20_N3	(25)					
		R345	15K_0402_5%		R348	15K_0402_5%					
USB4_P	W4	USB20_P4			USB20_P4	(20)			USB CAMERA		
USB4_N	W3	USB20_N4			USB20_N4	(20)					
		R347	15K_0402_5%		R344	15K_0402_5%					
USB5_P	W5	USB20_P5			USB20_P5	(30)			BLUETOOTH		
USB5_N	W6	USB20_N5			USB20_N5	(30)					
		R353	15K_0402_5%		R357	15K_0402_5%					
		BT@			BT@						
USB6_P	W7	USB20_P6			USB20_P6	(25)			MINI1		
USB6_N	W8	USB20_N6			USB20_N6	(25)					
		R360	15K_0402_5%		R358	15K_0402_5%					
		MINI1@			MINI1@						
USB7_P	Y2	USB20_P7			USB20_P7	(25)			MINI2		
USB7_N	Y3	USB20_N7			USB20_N7	(25)					
		R352	15K_0402_5%		R355	15K_0402_5%					
		MINI2@			MINI2@						
USB8_P	AA3	USB20_P8			USB20_P8	(26)			NEW CARD		
USB8_N	AA2	USB20_N8			USB20_N8	(26)					
		R350	15K_0402_5%		R356	15K_0402_5%					
		EXPRESS@			EXPRESS@						
USB9_P	AA5	USB20_P9			USB20_P9				NON-USE		
USB9_N	AA4	USB20_N9			USB20_N9						
		R351	15K_0402_5%		R354	15K_0402_5%					

HDA

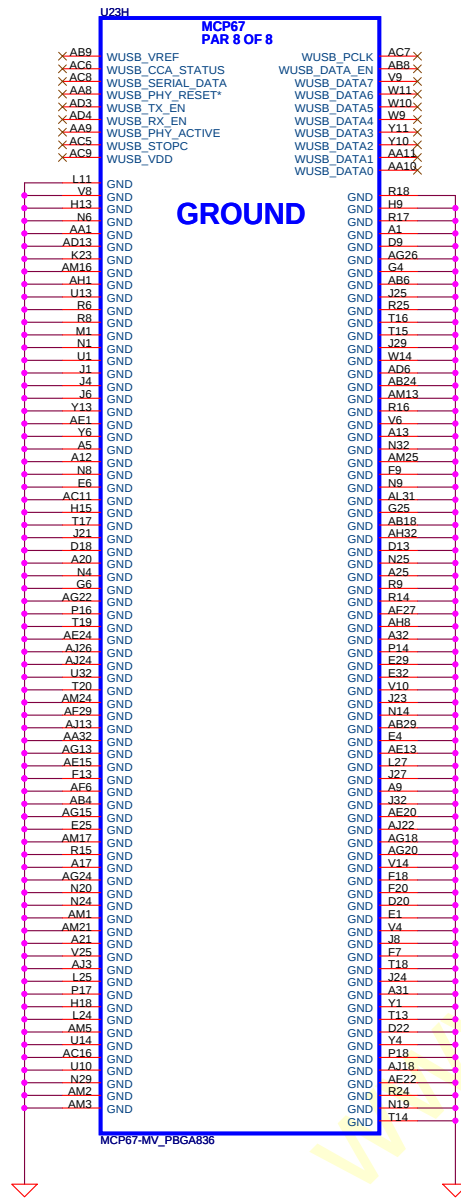


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				Custom	1.0
				Document Number ICW50 / ICY70 LA-3581P	
Date:		Friday, April 20, 2007	Sheet	14	of 42



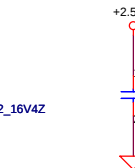
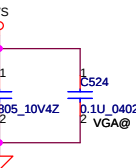
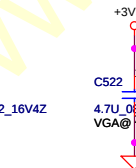
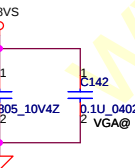
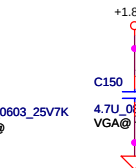
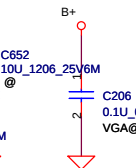
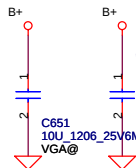
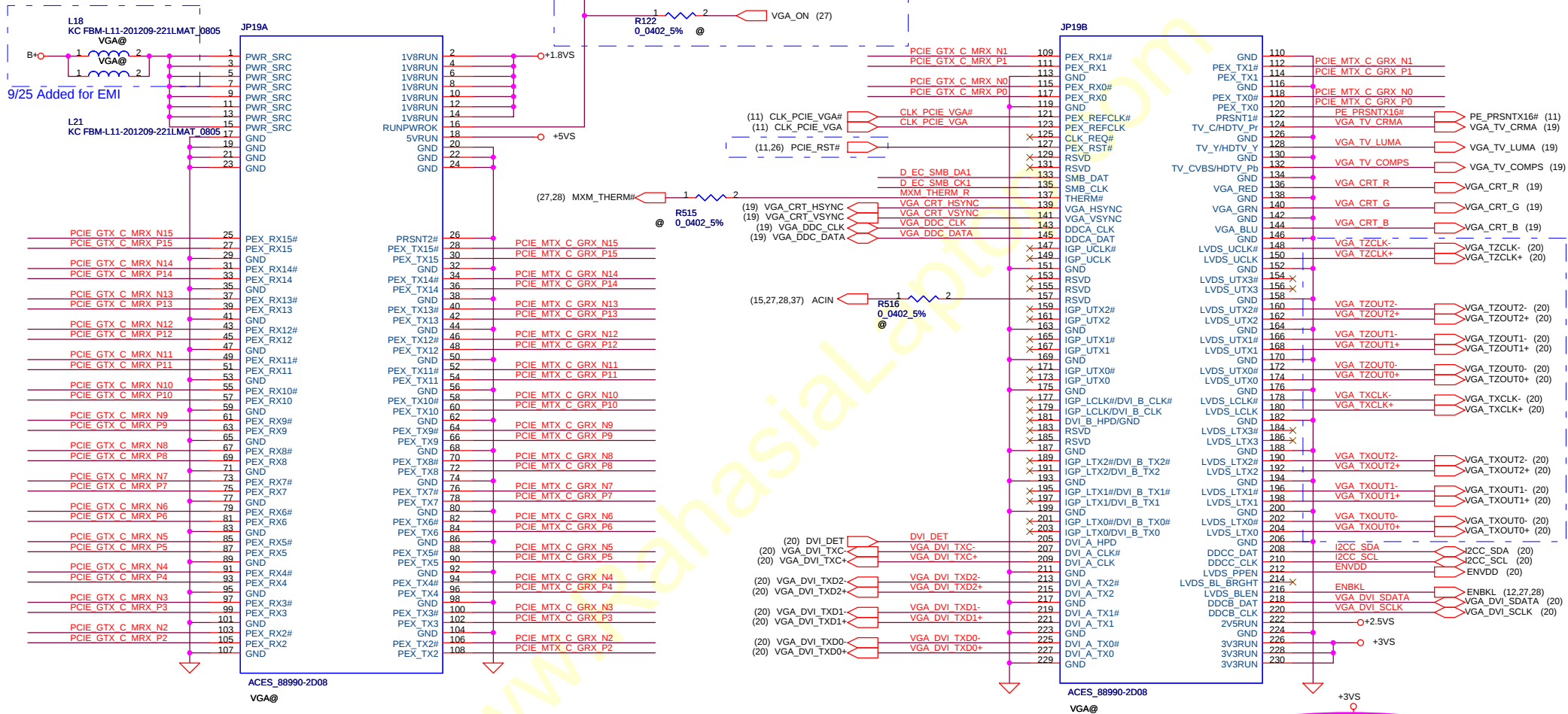
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Security Classification	Compal Secret Data			Title MCP67 POWER
Issued Date	2006/08/18	Deciphered Date	2007/8/18	
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Size Custom	Document Number ICW50 / ICY70 LA-3581P			Rev 1.0
Date:	Friday, April 20, 2007		Sheet 16 of 42	

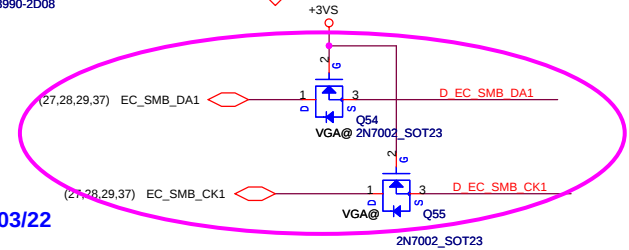


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				MCP67 GROUND	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom	1.0
Date: Friday, April 20, 2007		Sheet 17 of 42			

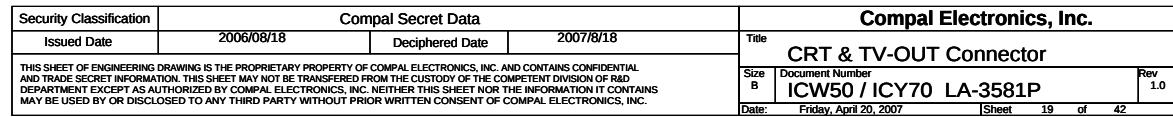
- (11) PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15]
(11) PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15]
(11) PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]
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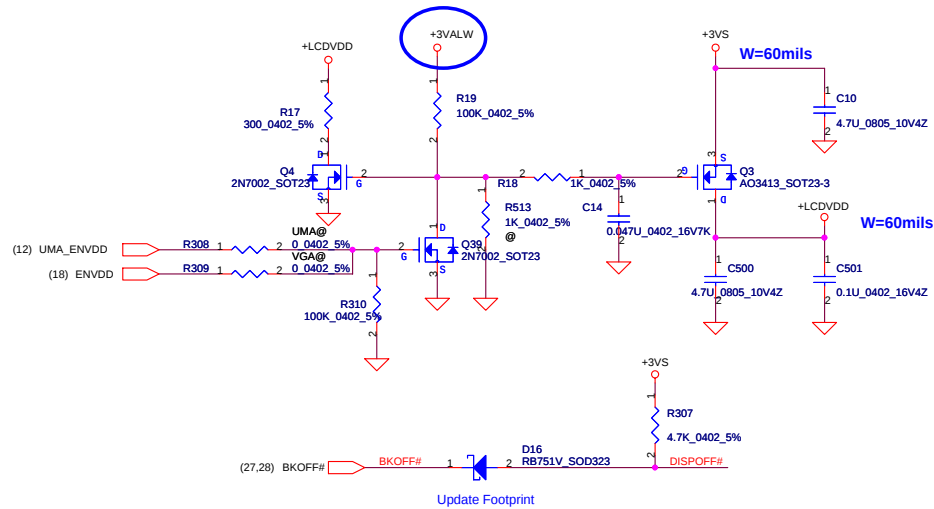
PVT Modify 2007/03/22



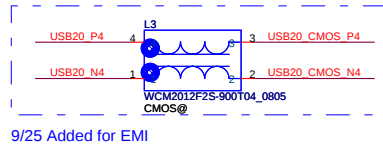
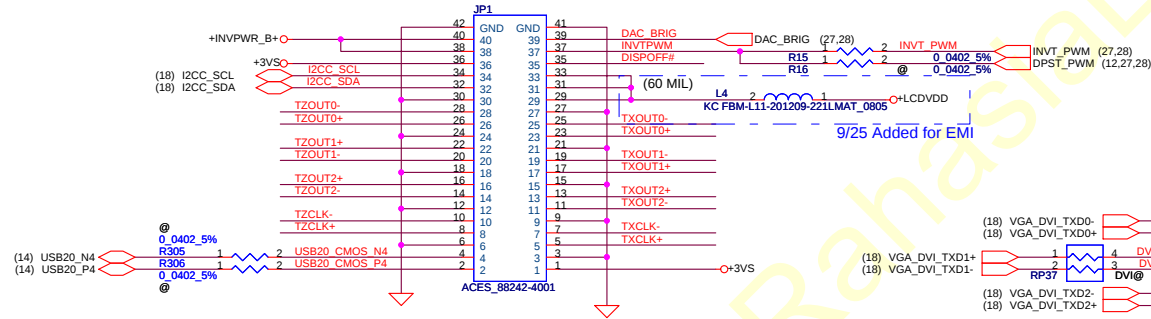
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Size B	Document Number
				ICW50 / ICY70 LA-3581P	
Date: Friday, April 20, 2007		Sheet 18		of 42	
				Rev 1.0	

TV-OUT Conn.

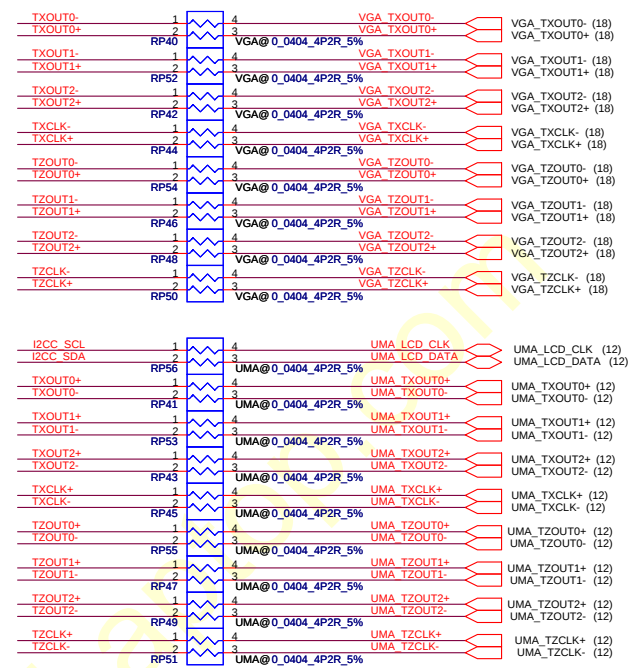
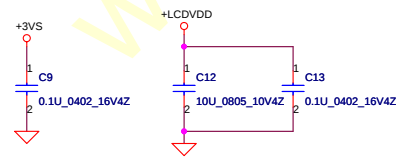
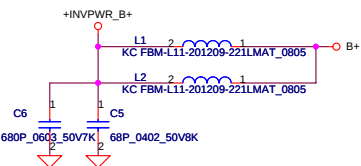
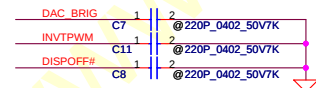
LCD POWER CIRCUIT



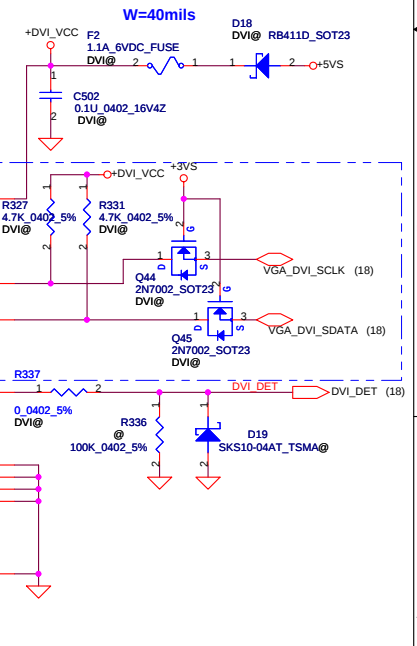
LCD/PANEL BD. Conn.



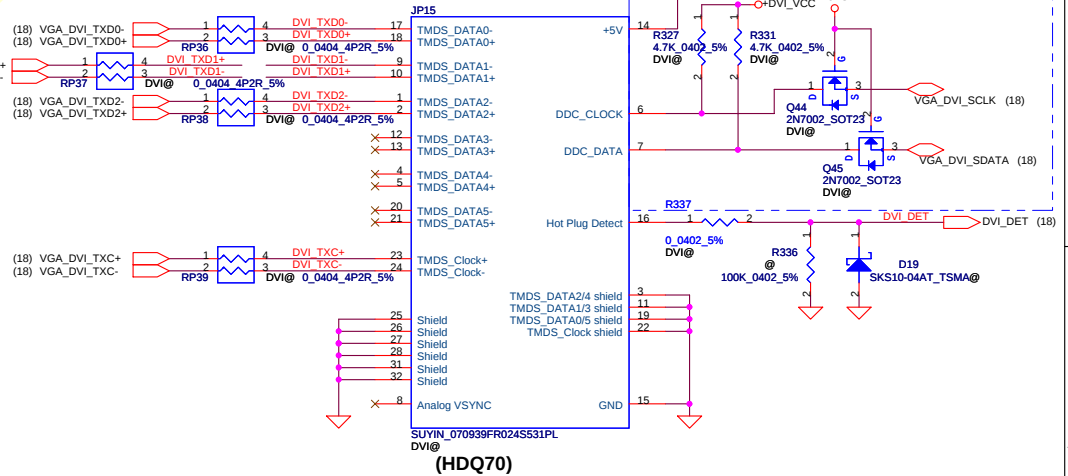
Fro CMOS Camera



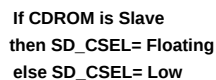
10/2 SWAP PIN



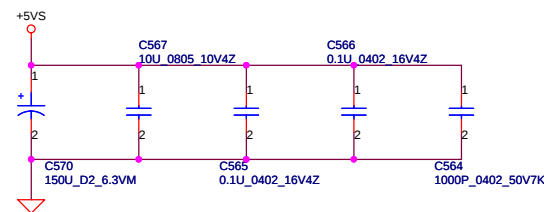
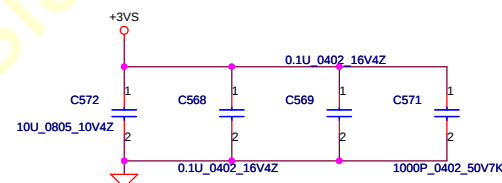
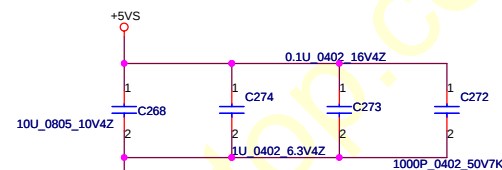
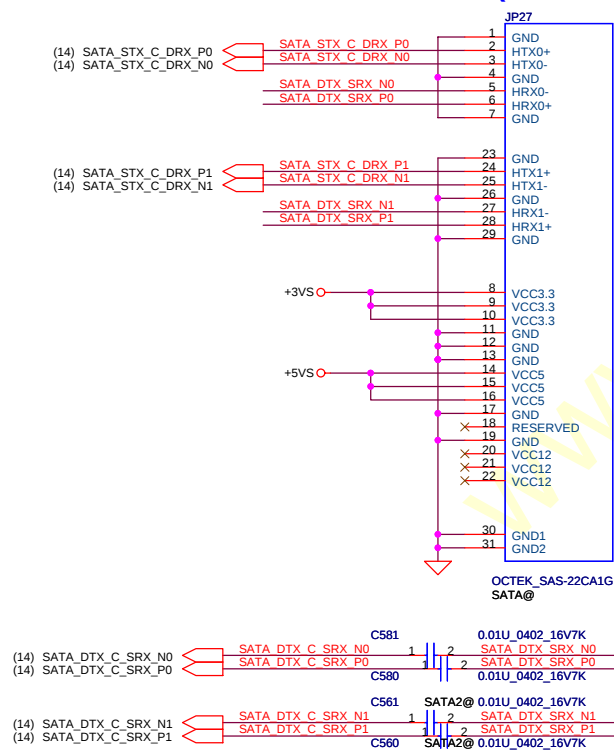
DVI-D Connector



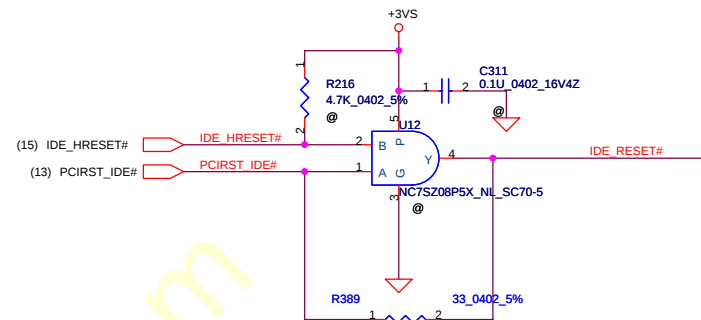
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	LVDS & DVI Connector
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				B	ICW50 / ICY70 LA-3581P
				Rev	1.0
Date:				Friday, April 20, 2007	Sheet 20 of 42



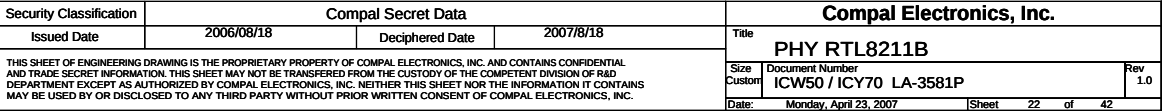
SATA HDD Conn.(SAS Connector)

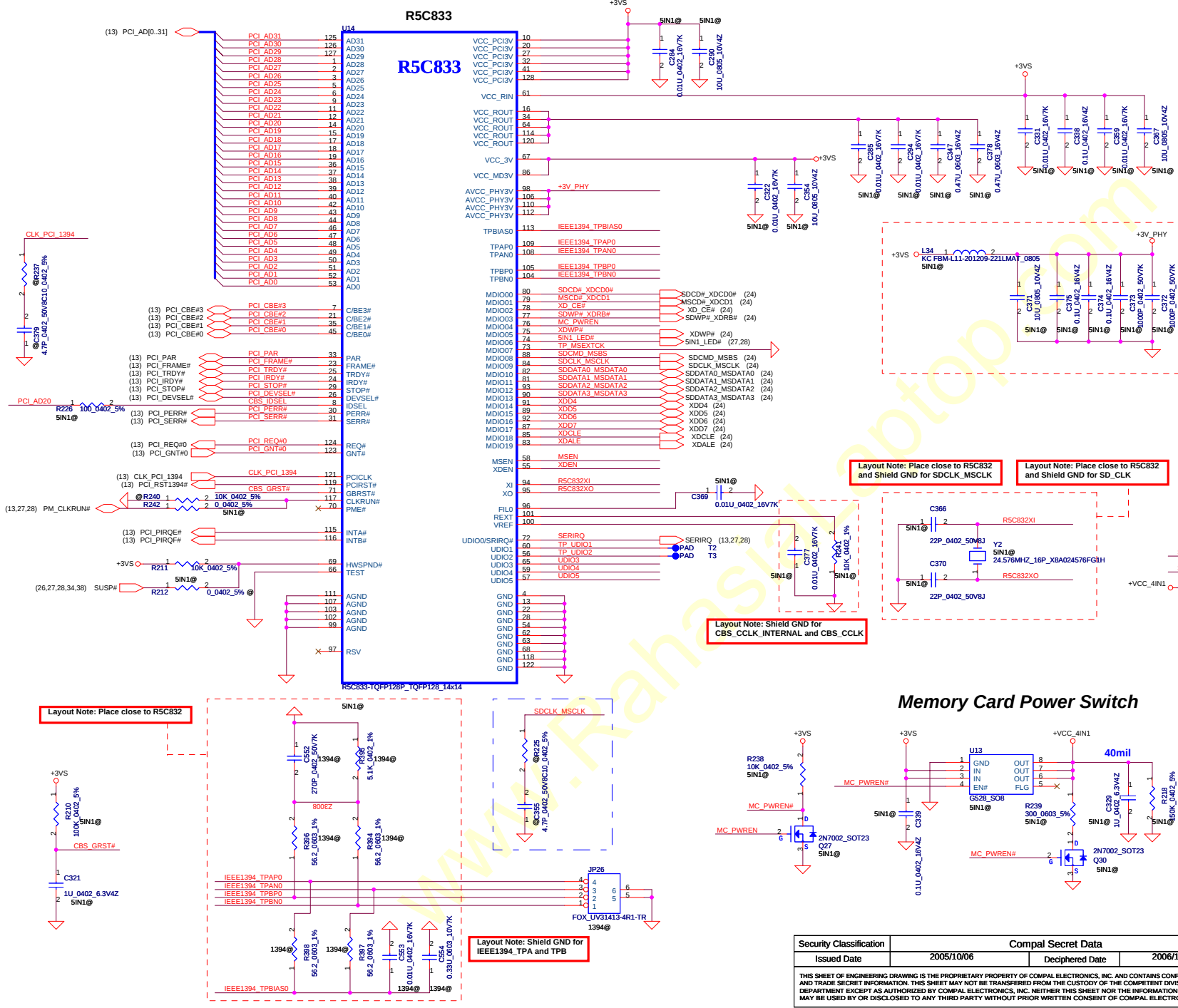


Close to SATA HDD



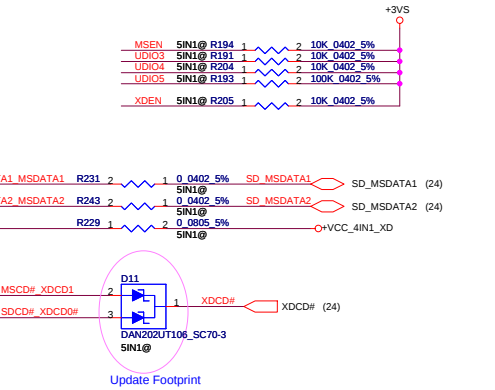
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	SATA HDD & IDE ODD Connector
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				Date	ICW50 / ICY70 LA-3581P
				Rev	1.0
				Sheet	21 of 42





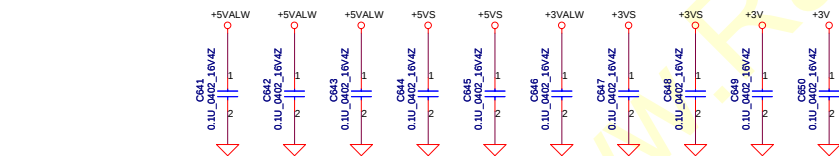
SD, MMC, MS, XD multi-function pin define				
MDIO PIN Name	SD Card PIN Name	MMC Card PIN Name	MS Card PIN Name	XD Card PIN Name
MDIO00	SDCD#	MMCCD#		XDCD0#
MDIO01			MSCD#	XDCD1#
MDIO02				XDCE#
MDIO03	SDWP#			XDR/B#
MDIO04	SDPWR0	MMCPWR	MSWR	XDPCR
MDIO05	SDPWR1			XDWP#
MDIO06	SDLED#	MMCLD#	MSLED#	XDLED#
MDIO07				
MDIO08	SDCCMD	MMCCMD	MSBS	XDWE#
MDIO09	SDCLK	MMCLK	MSCLK	XDRE#
MDIO10	SDCDAT0	MMCDAT	MSDAT0	XDCDAT0
MDIO11	SDCDAT1		MSDAT1	XDCDAT1
MDIO12	SDCDAT2		MSDAT2	XDCDAT2
MDIO13	SDCDAT3		MSDAT3	XDCDAT3
MDIO14				XDCDAT4
MDIO15				XDCDAT5
MDIO16				XDCDAT6
MDIO17				XDCDAT7
MDIO18				XDCL
MDIO19				XDAL

Function set pin define				
UDIO3	UDIO4	MSEN	XDEN	Function
Pull-up	Pull-up	Pull-up	Pull-up	Enable SD, XD, MS, MMC Card



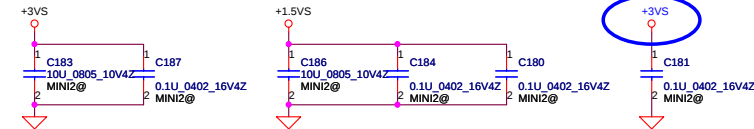
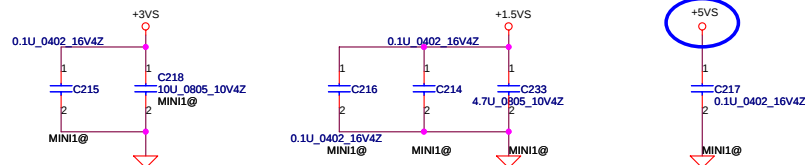
Memory Card Power Switch

Security Classification		Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date	2006/10/06
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Title		Compal Electronics, Inc.	
R5C833 1394+Card reader		Rev 1.0	
Size	Document Number	ICW50 / ICY70 LA-3581P	
Custom	Date	Friday, April 20, 2007	Sheet 23 of 42

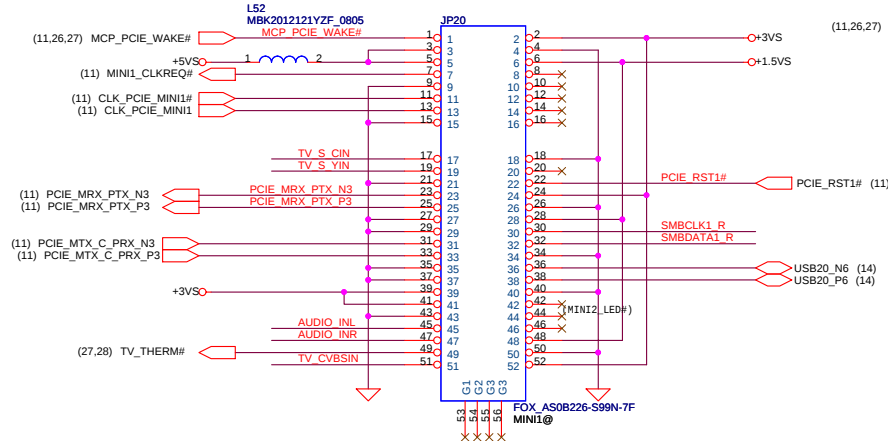


```
H1          : H_C236BC315D138
H6,H7,H16,H17 : H_C315BC168D165
H25,H26      : H_C236D98
H31,H32,H33  : H_C236BC131D128
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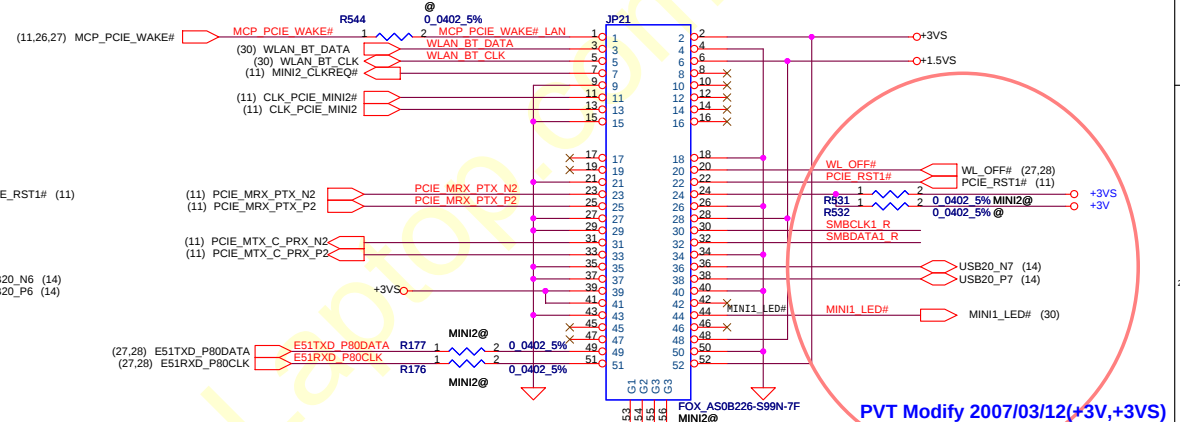
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title	Card Reader Conn / Screw	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	ICW50 / ICY70 LA-3581P	1.0
				Date:	Friday, April 20, 2007	Sheet 24 of 42



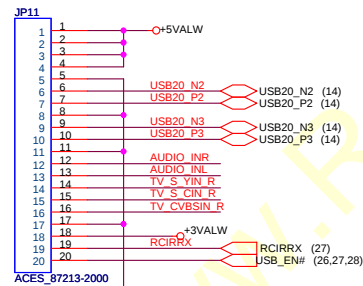
TV TUNNER



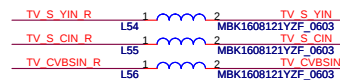
PVT2 Modify 2007/04/12



USB/B Connector



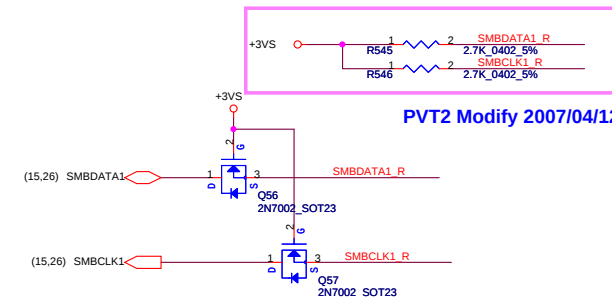
AV-IN Connector CIR



EMI PVT Modify 2007/03/12 Close JP11

Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

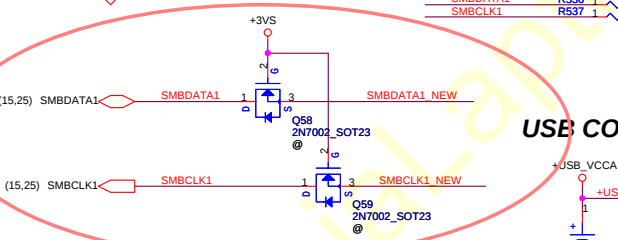
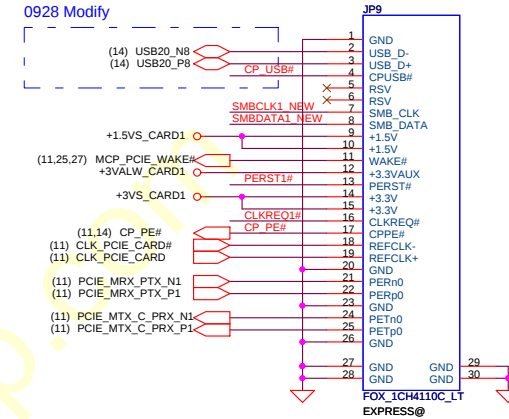
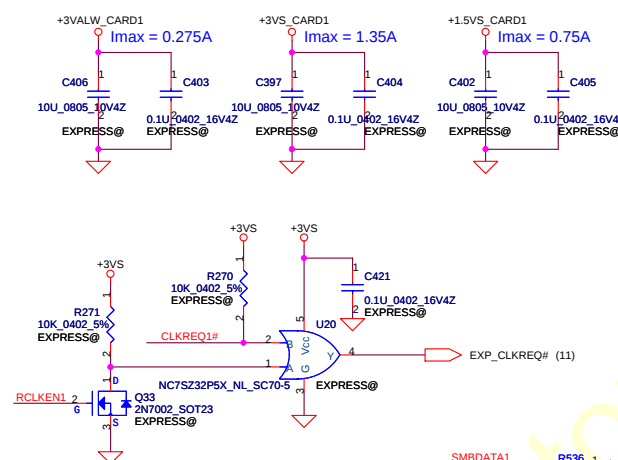
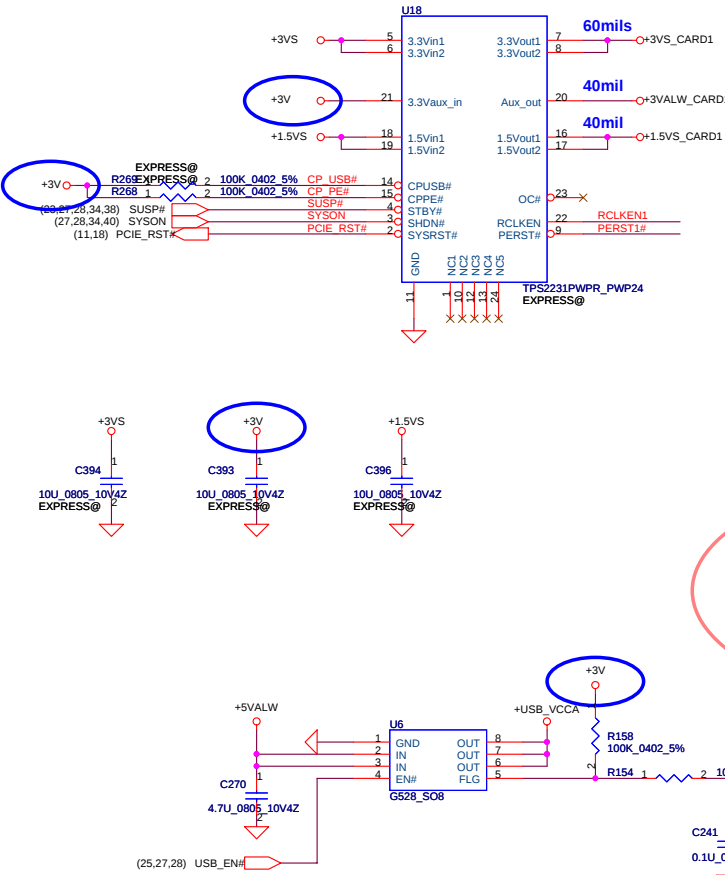
PVT2 Modify 2007/04/12



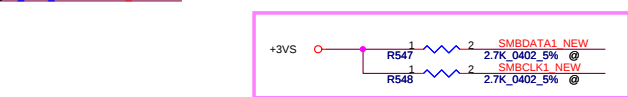
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	MINI CARD / USB-B Conn.
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				Date	Friday, April 20, 2007
				Sheet	25 of 42
				Rev	1.0
				ICW50 / ICY70	LA-3581P

New Card Power Switch

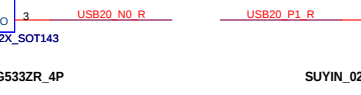
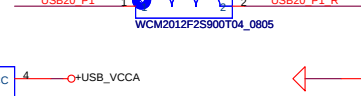
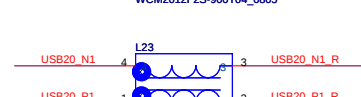
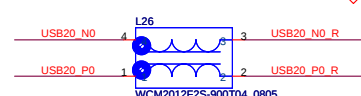
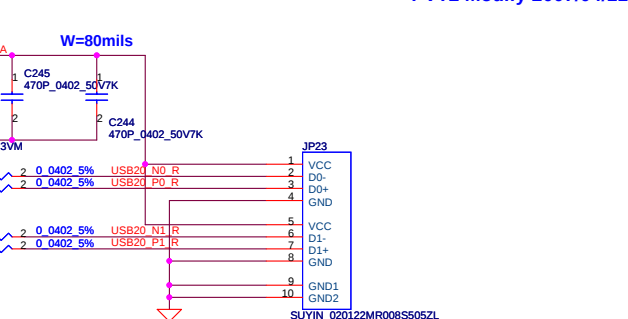
New Card Socket (Left/TOP)



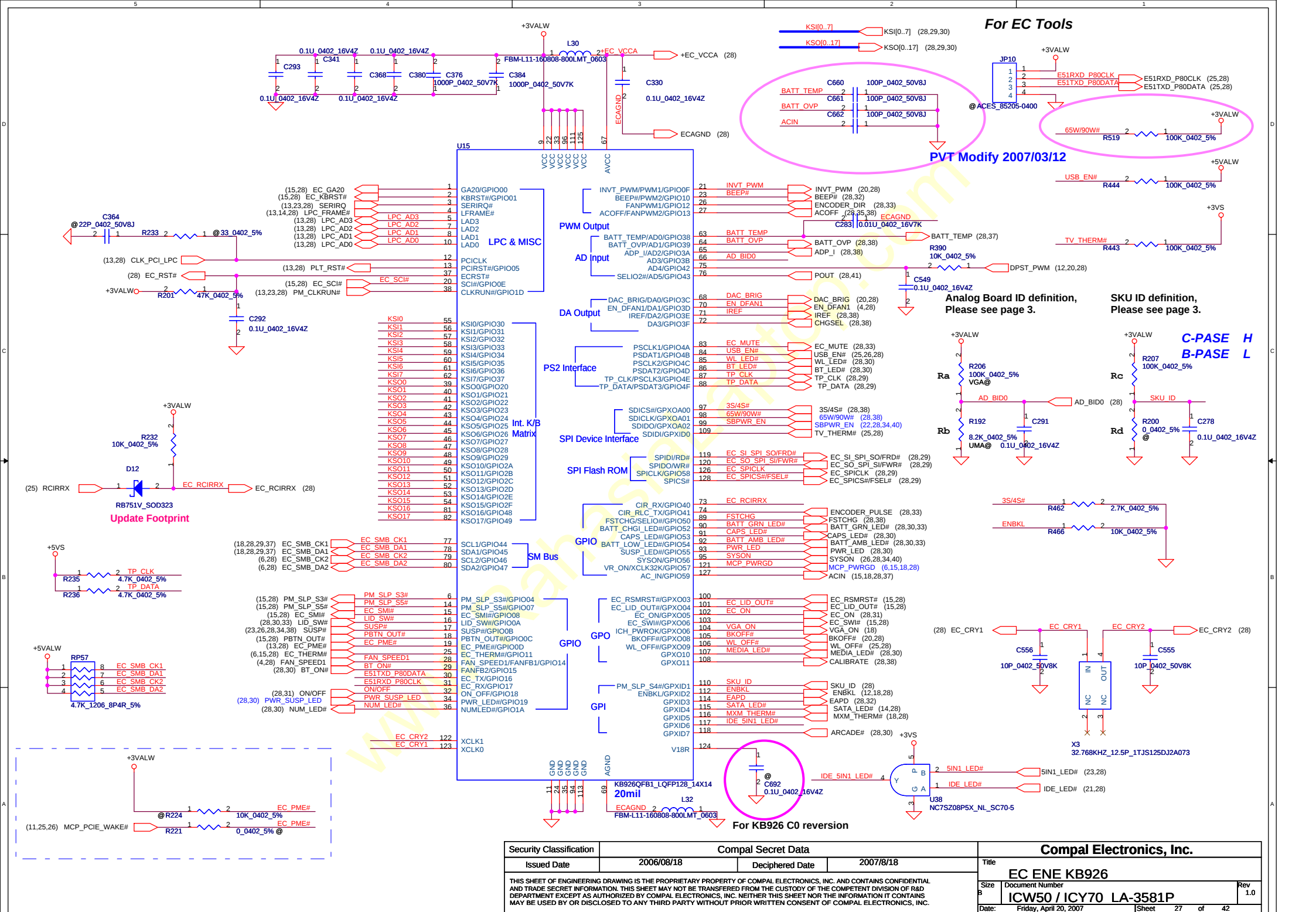
USB CONN. 1(Stack-up Type)



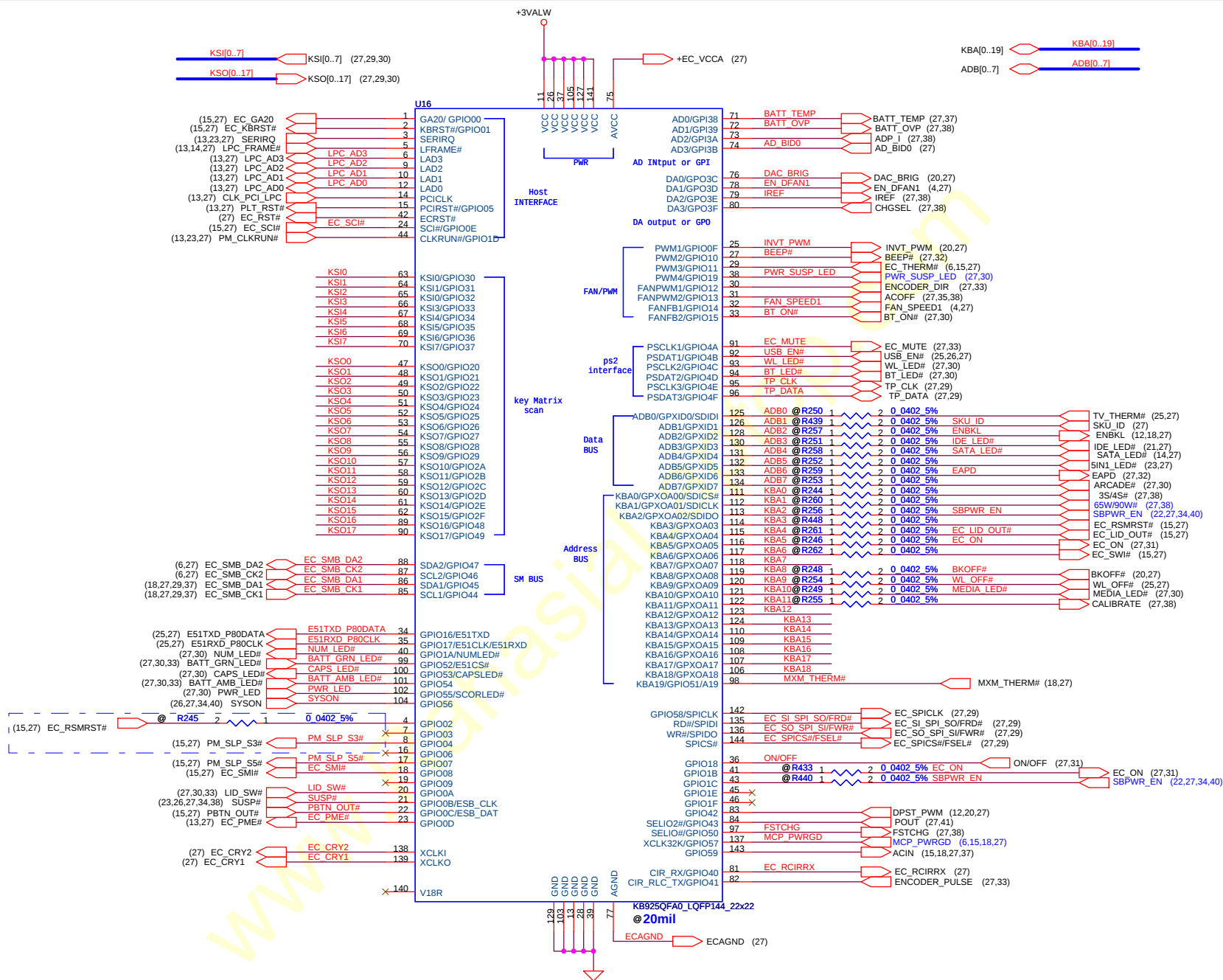
PVT2 Modify 2007/04/11



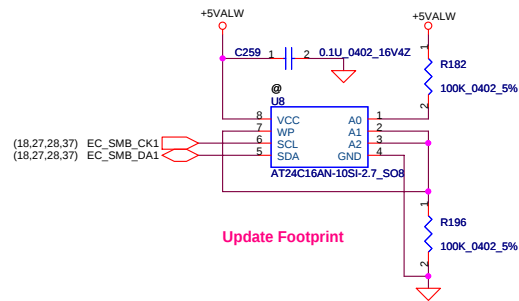
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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SUYIN_020173MR004G533ZR_4P				Size B	Rev 1.0
SUYIN_020173MR004G533ZR_4P				Document Number	ICW50 / ICY70 LA-3581P
SUYIN_020173MR004G533ZR_4P				Date: Friday, April 20, 2007	Sheet 26 of 42



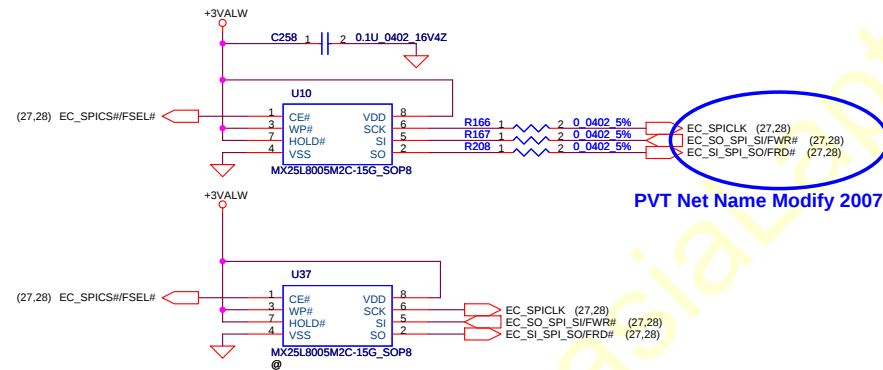
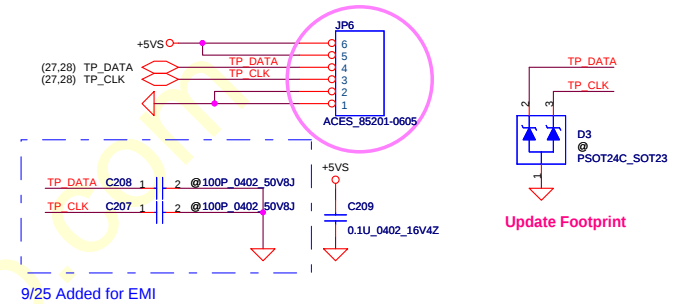
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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Size	Document Number	Rev		Date	
3	ICW50 / ICY70 LA-3581P	1.0		Friday, April 20, 2007	
Sheet		27		of 42	



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18		Deciphered Date		2007/8/18		Title	
										EC ENE KB910L/925(Reserved)	
										Rev	
										1.0	
										Date:	
										Friday, April 20, 2007	
										Sheet	
										28	
										of	
										42	

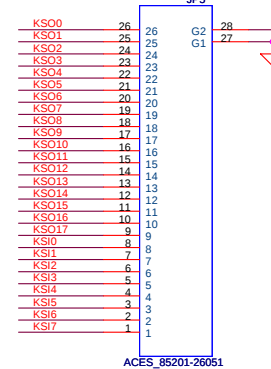


To TP/B Conn.

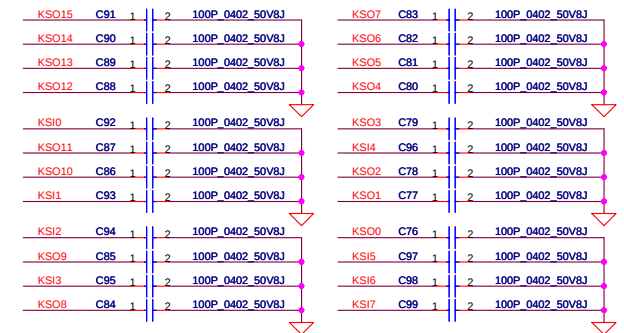


INT_KBD Conn.

(Left)



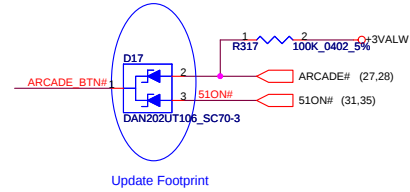
(Right)



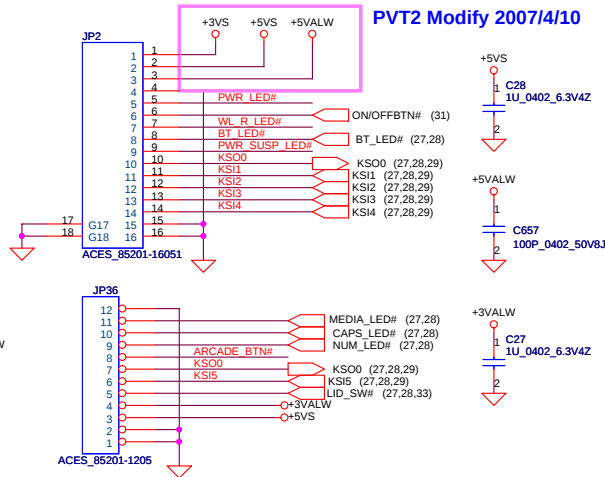
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2006/08/18				Deciphered Date			
2007/8/18				2007/8/18				Title			
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								Document Number			
								ICW50 / ICY70 LA-3581P			
								Date:			
								Monday, April 23, 2007			
								Sheet			
								29 of 42			
								Rev			
								1.0			

	KSO0
KS11	WL_BTN#
KS12	BT_BTN#
KS13	EMAIL_BTN#
KS14	IE_BTN#
KS15	E-KEY_BTN#

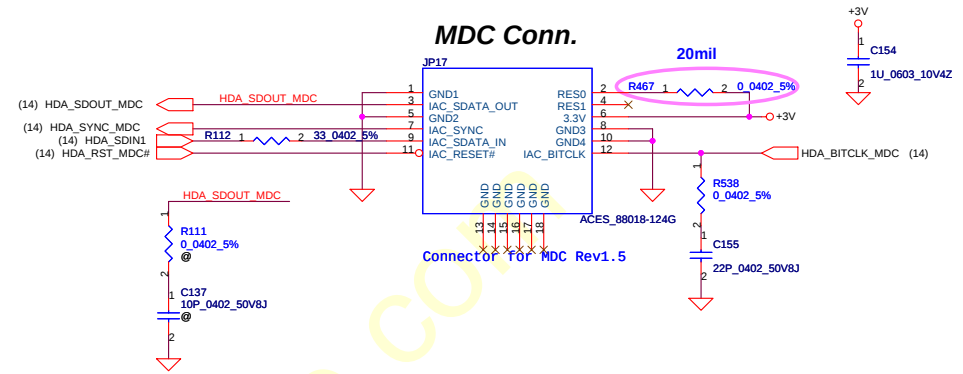
Check 15.4" K/B Matrix



PVT2 Modify 2007/4/10

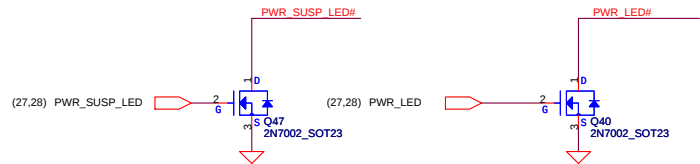
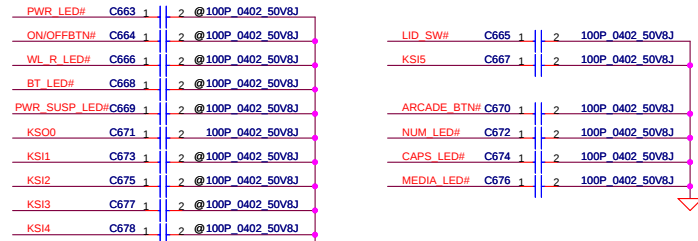


MDC Conn.

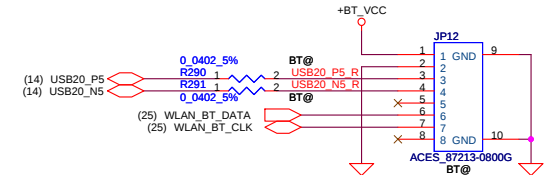
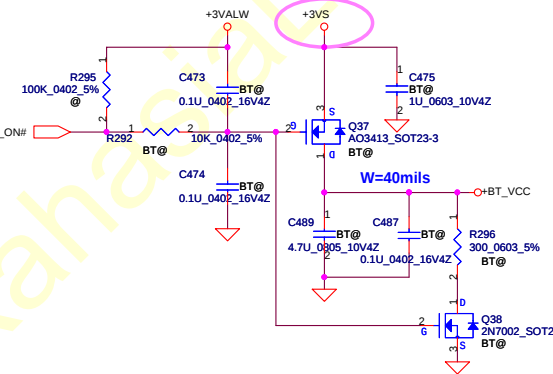


Connector for MDC Rev1.5

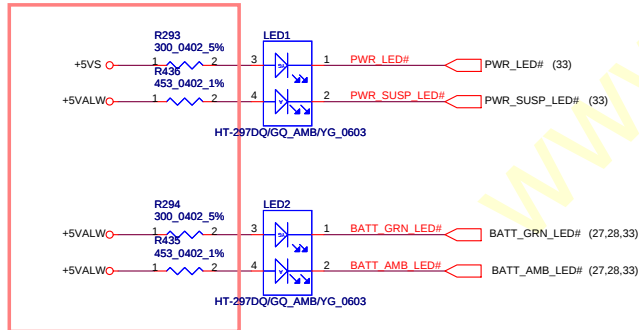
EMI PVT Modify 2007/3/12



Bluetooth Conn.



9/25 Added for EMI

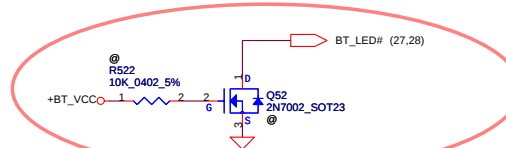


PVT Value Modify to 453E 2007/3/12

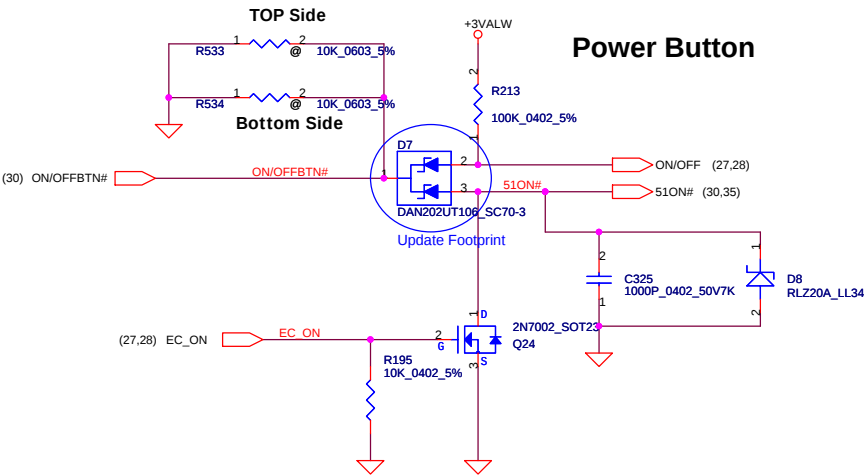
Compal Footprint

4 2
3 1

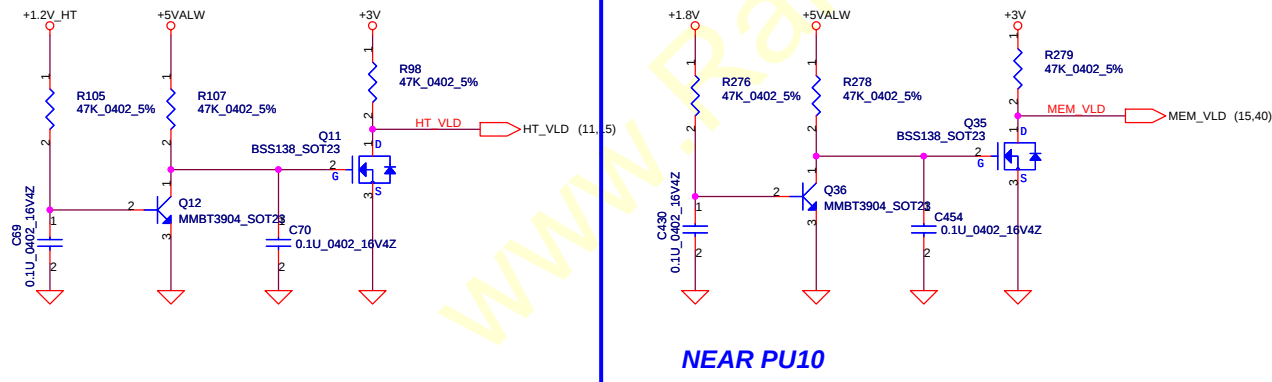
PVT Modify 2007/3/12



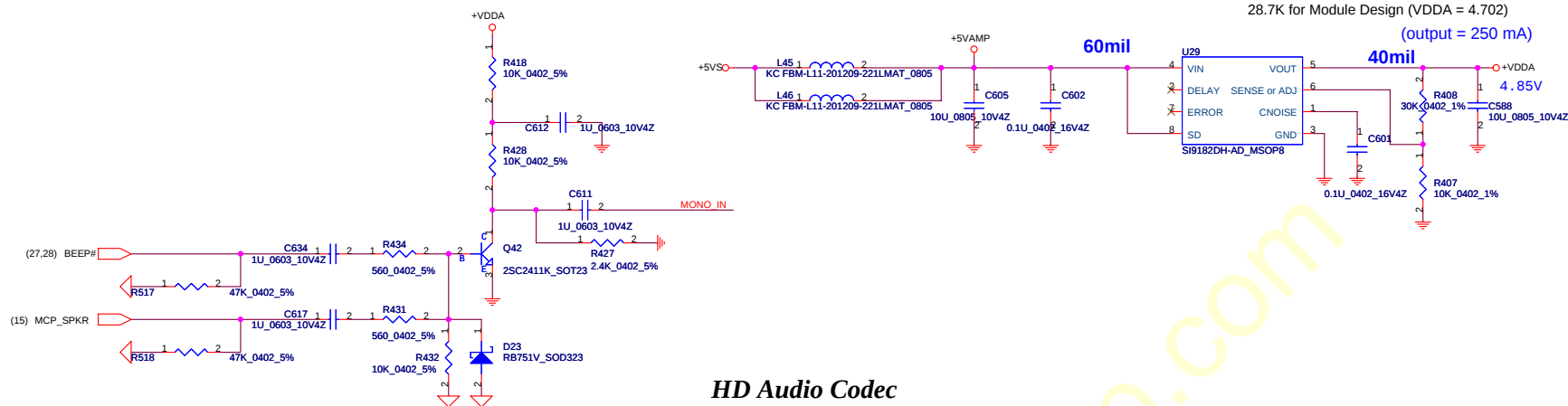
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	MDC / BT / CIR / LED
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				ICW50 / ICY70	LA-3581P
				Date: Friday, April 20, 2007	Sheet 30 of 42



Power ON Circuit

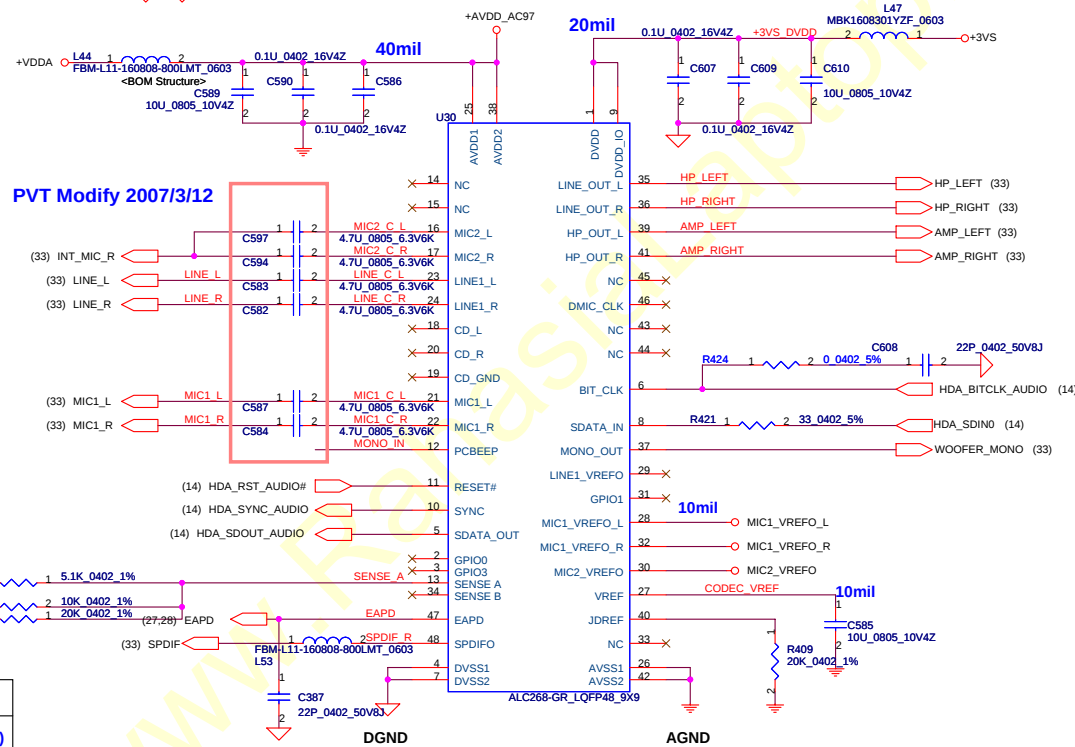


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				Date: Friday, April 20, 2007	Rev 1.0
				Sheet 31 of 42	

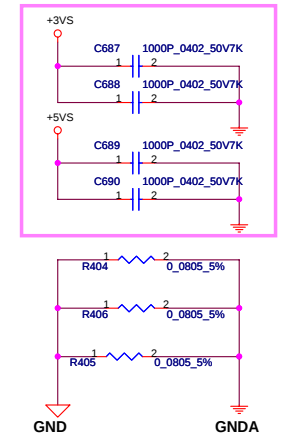


HD Audio Codec

PVT Modify 2007/3/12

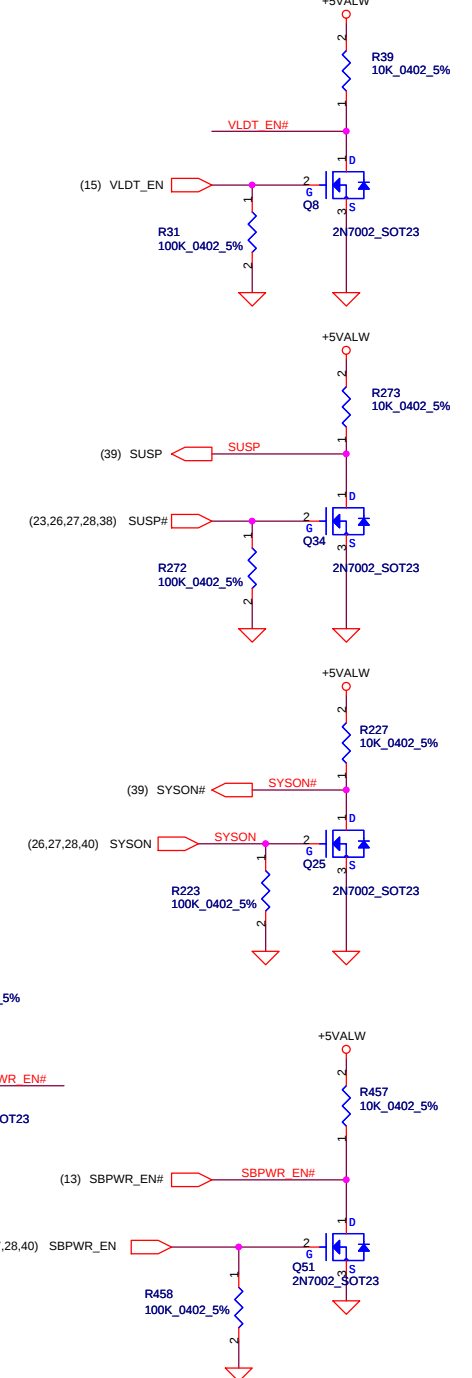
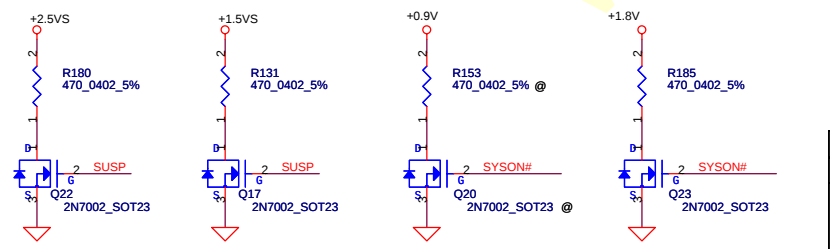
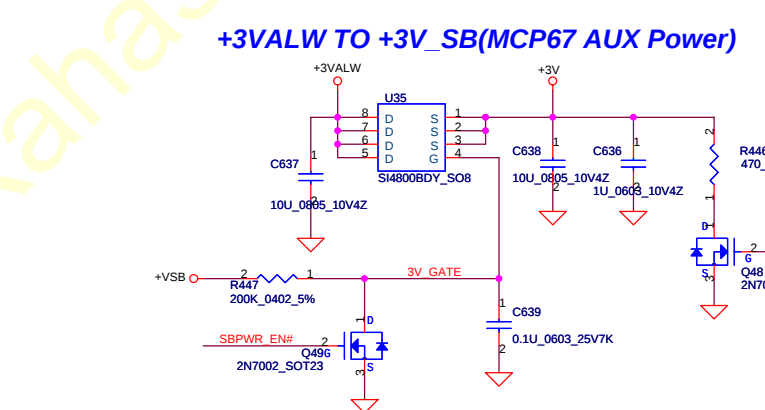
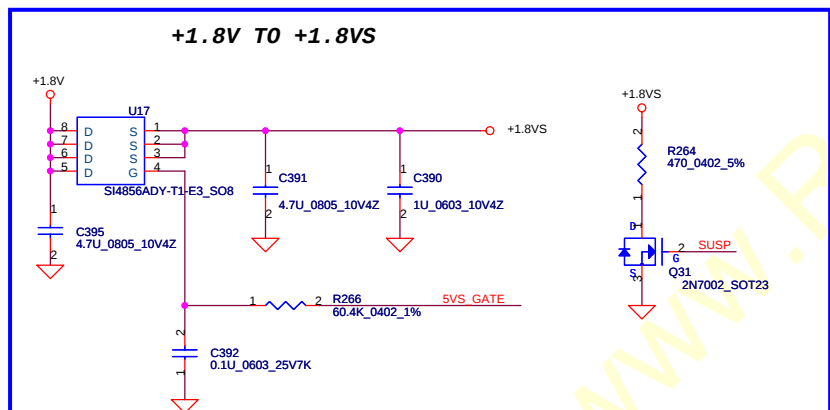
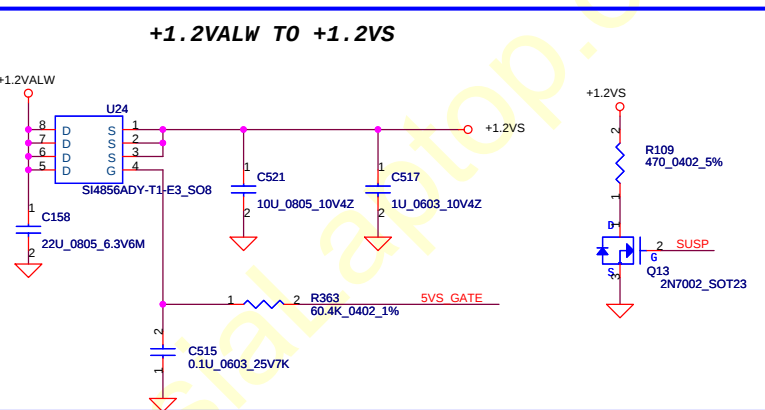
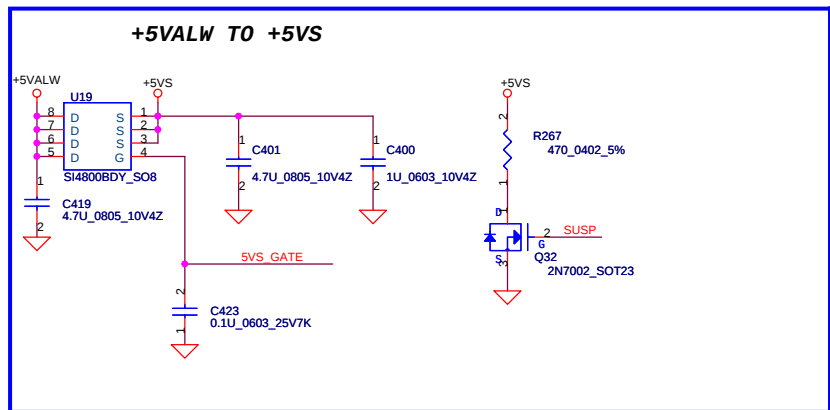
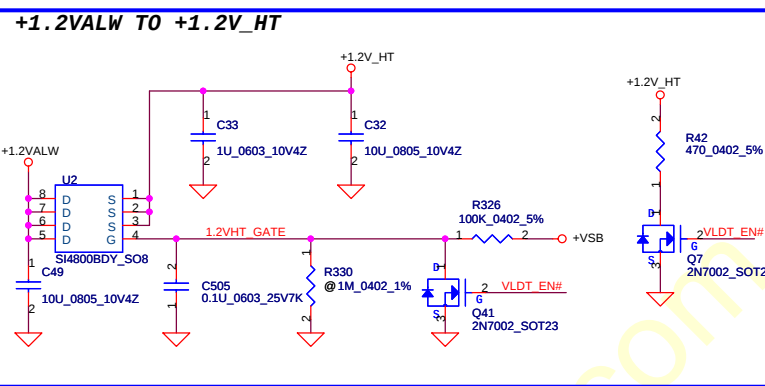
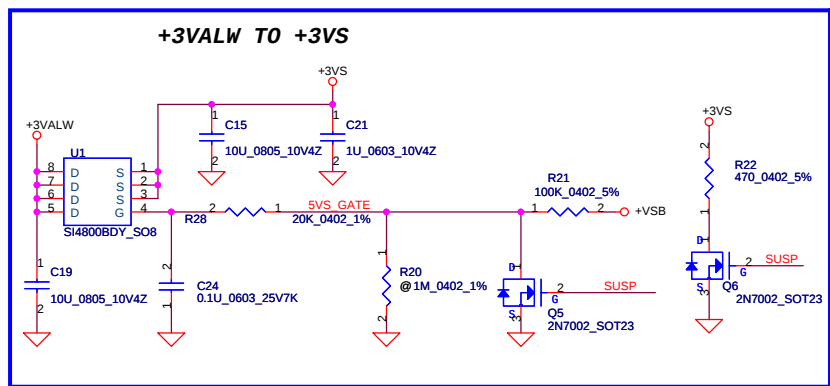


EMI Added 2007/4/12

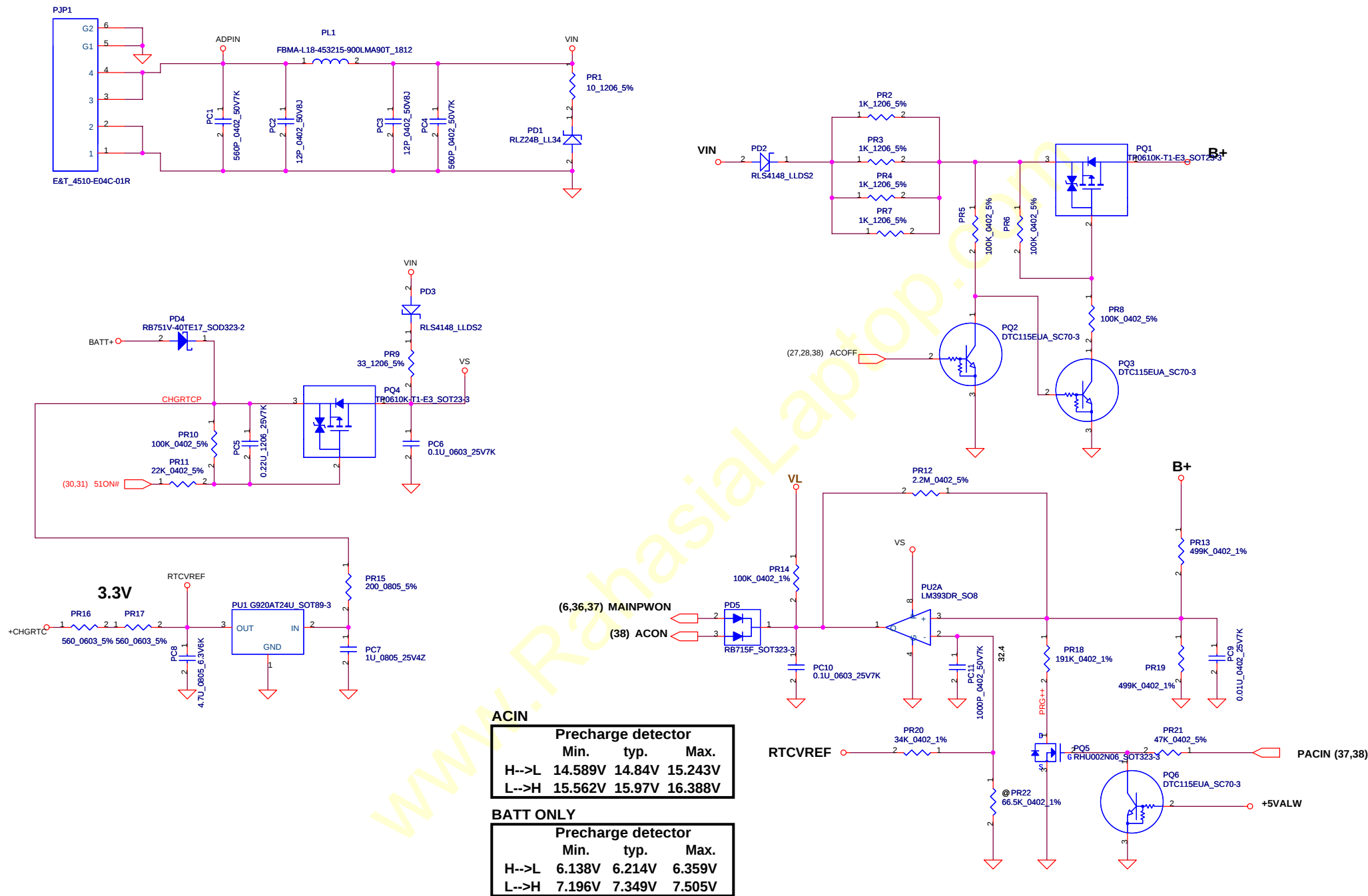


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

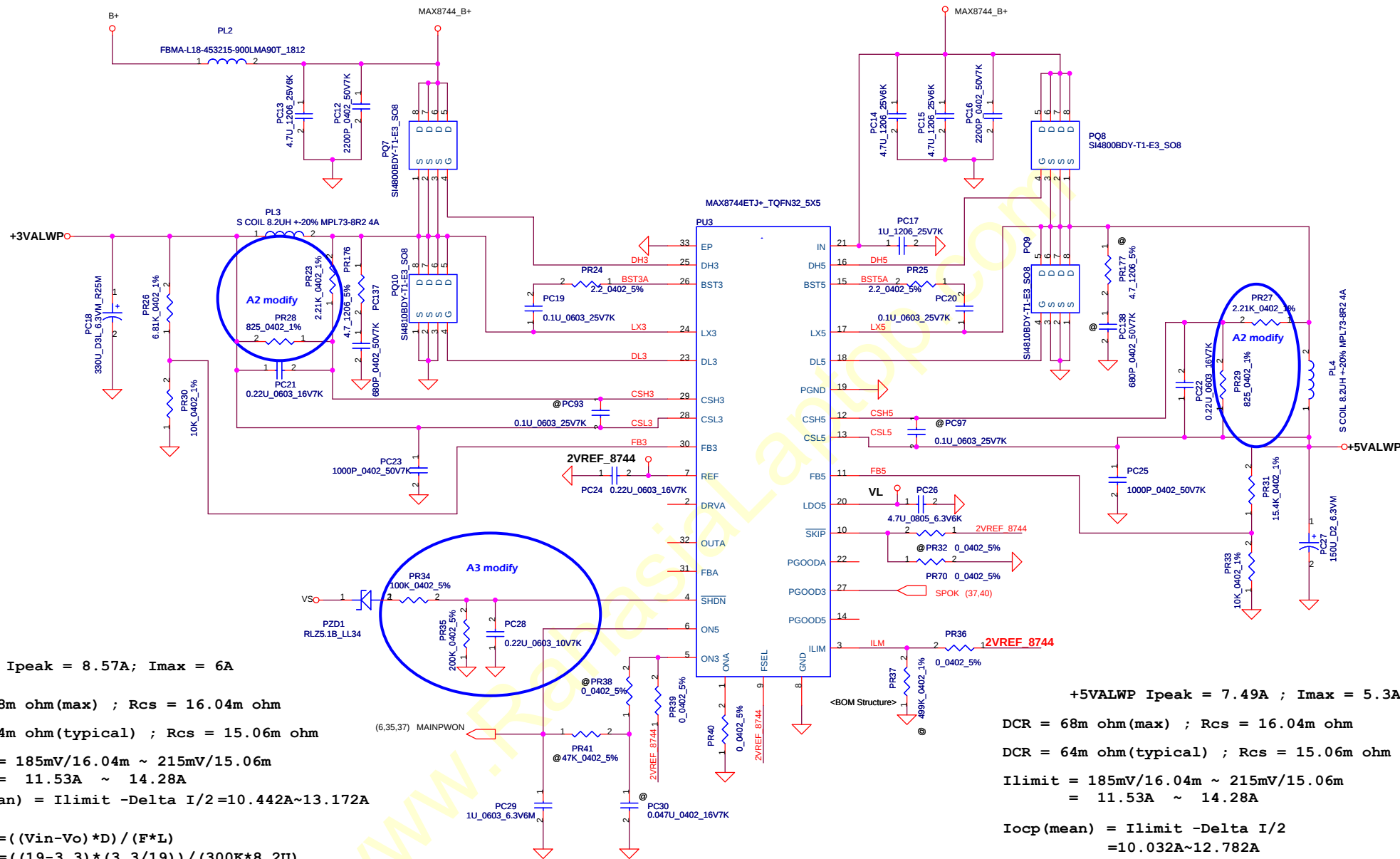
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				Date: Friday, April 20, 2007	Rev 1.0
				ICW50 / ICY70 LA-3581P	Sheet 32 of 42



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						DC INTERFACE	
						Size	Document Number
Date		ICW50 / ICY70 LA-3581P				1.0	
a		Friday, April 20, 2007				Sheet 34 of 42	



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				Date: Friday, April 20, 2007	Sheet 35 of 42



+3VALWP Ipeak = 8.57A; Imax = 6A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m
= 11.53A ~ 14.28A

Iocp(mean) = Ilimit -Delta I/2=10.442A~13.172A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-3.3)*(3.3/19))/(300K*8.2U)
=1.108A

Notes :

fESR<=fOSC/n ; fESR=1/(2*π*RESR*COU2)

ON3 = REF --->3.3V starts up delay 2ms after 5V starts up

+5VALWP Ipeak = 7.49A ; Imax = 5.3A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

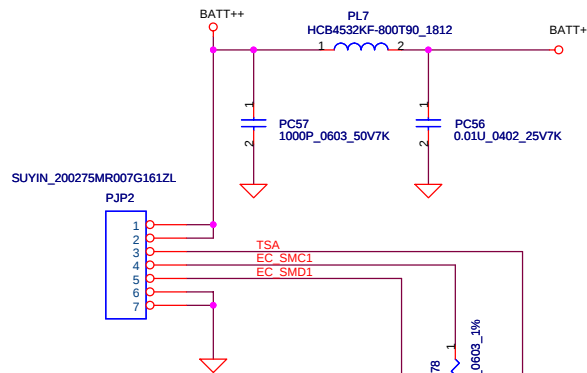
DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m
= 11.53A ~ 14.28A

Iocp(mean) = Ilimit -Delta I/2
=10.032A~12.782A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-5)*(5/19))/(300K*8.2U)
=1.498A

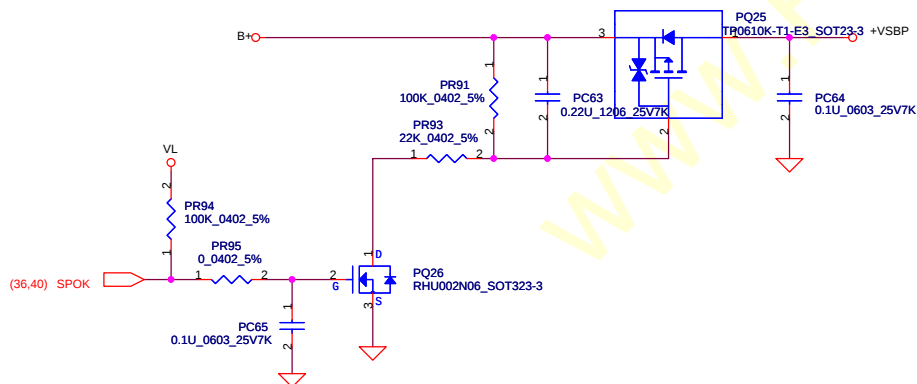
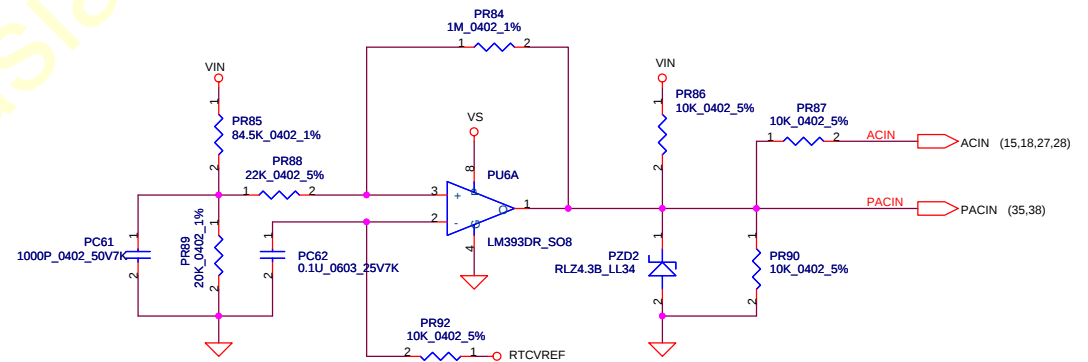
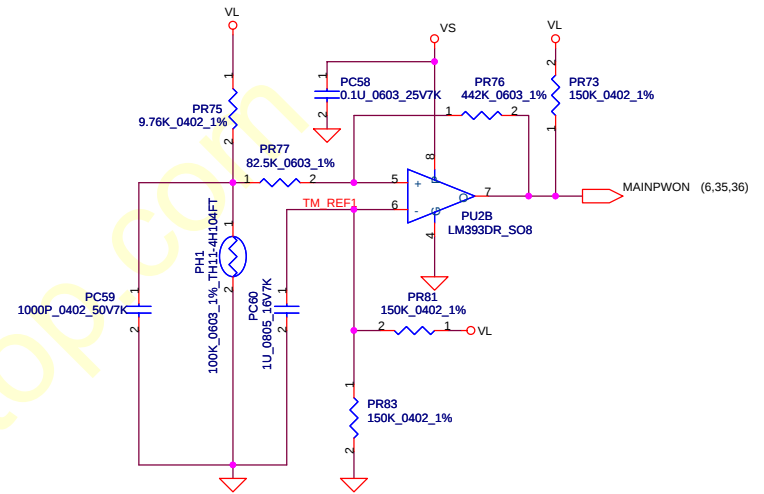
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										Custom		ICW50/ICX70		1.0					
										Date:		Friday, April 20, 2007				Sheet		36 of 42	



PJP2 battery connector

SMART
Battery:
1.BATT+
2.BATT+
3.TS
4.SMC
5.SMD
6.GND
7.GND

PH1 under CPU bottom side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C



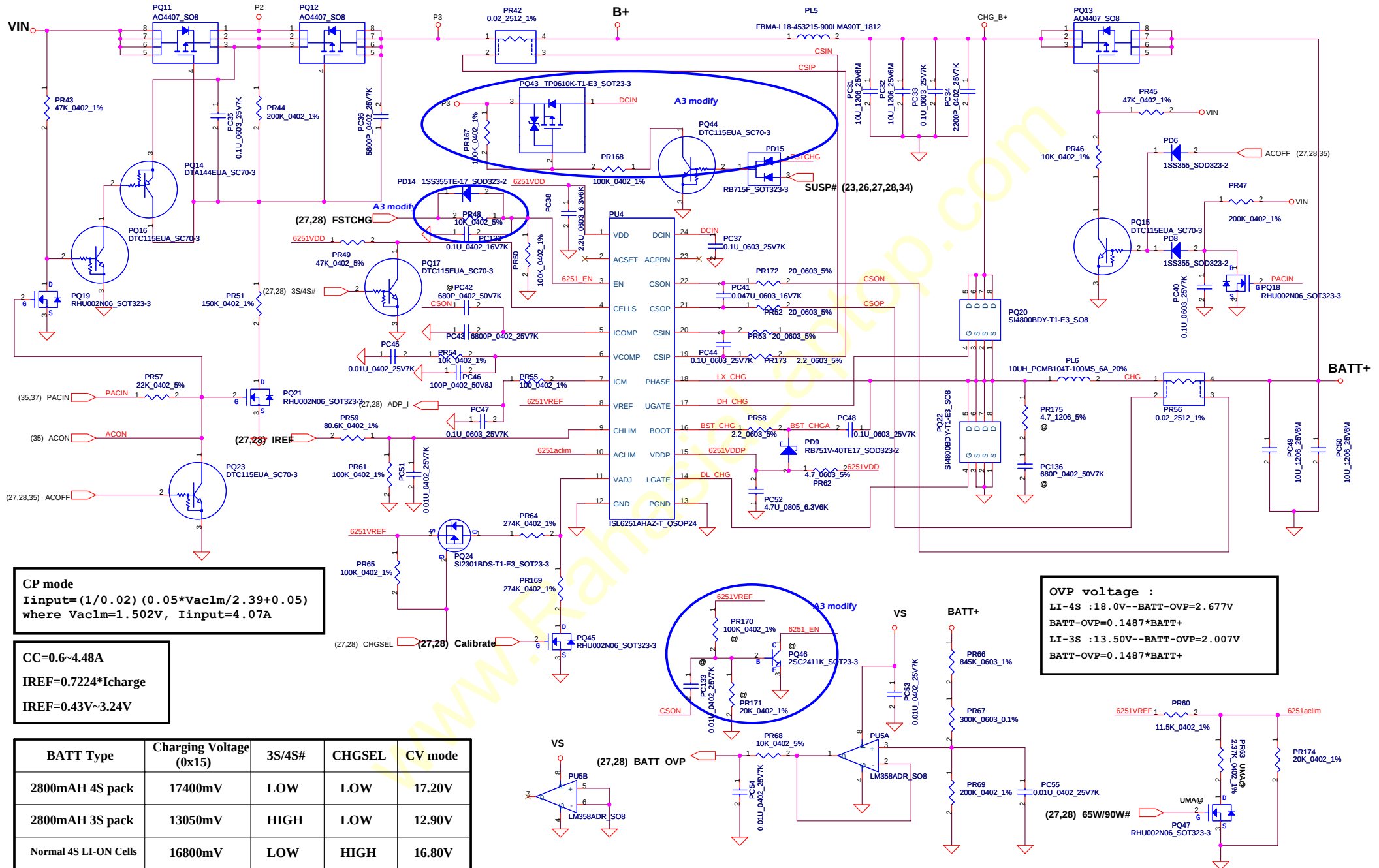
Vin Detector		
Min.	typ.	Max.
H-->L	16.976V	17.257V
L-->H	17.430V	18.384V

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				Date: Friday, April 20, 2007	Sheet 37 of 42

Iada=0~4.74A (90W)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 1.502V$, $I_{input} = 4.07A$

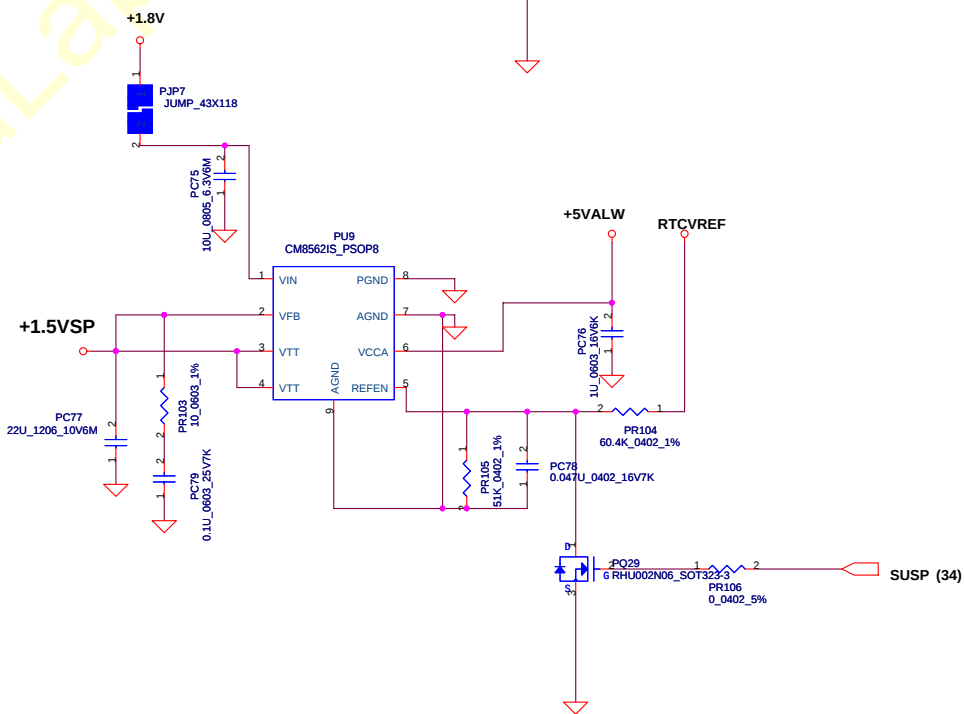
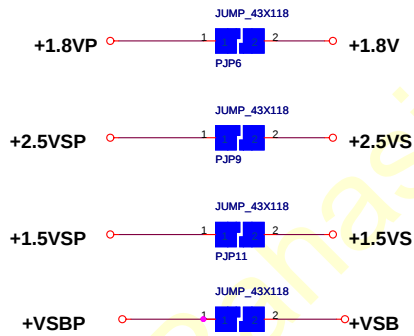
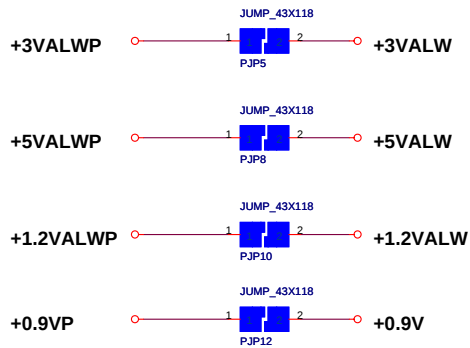
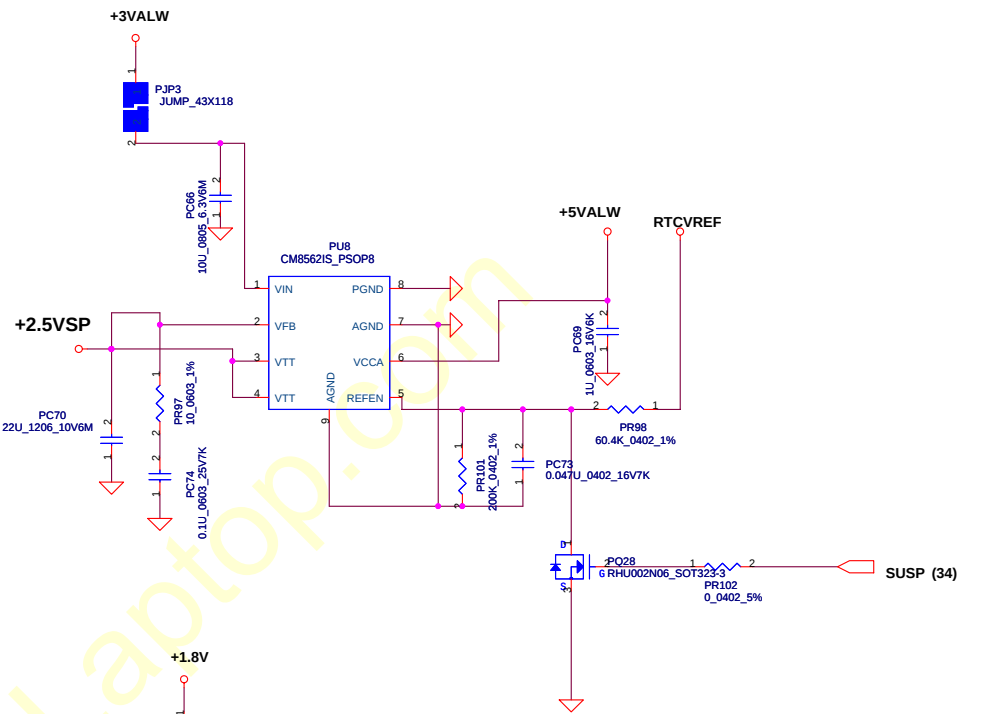
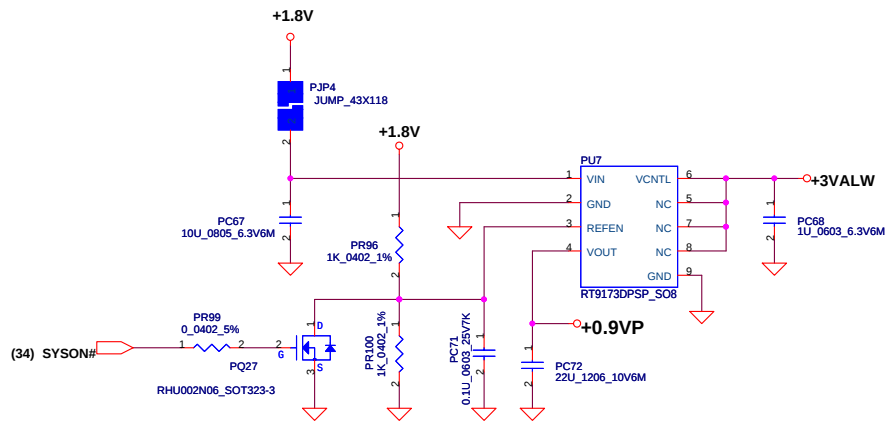
CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

OVP voltage :
 LI-4S : 18.0V -- BATT-OVP = 2.677V
 BATT-OVP = 0.1487 * BATT+
 LI-3S : 13.50V -- BATT-OVP = 2.007V
 BATT-OVP = 0.1487 * BATT+

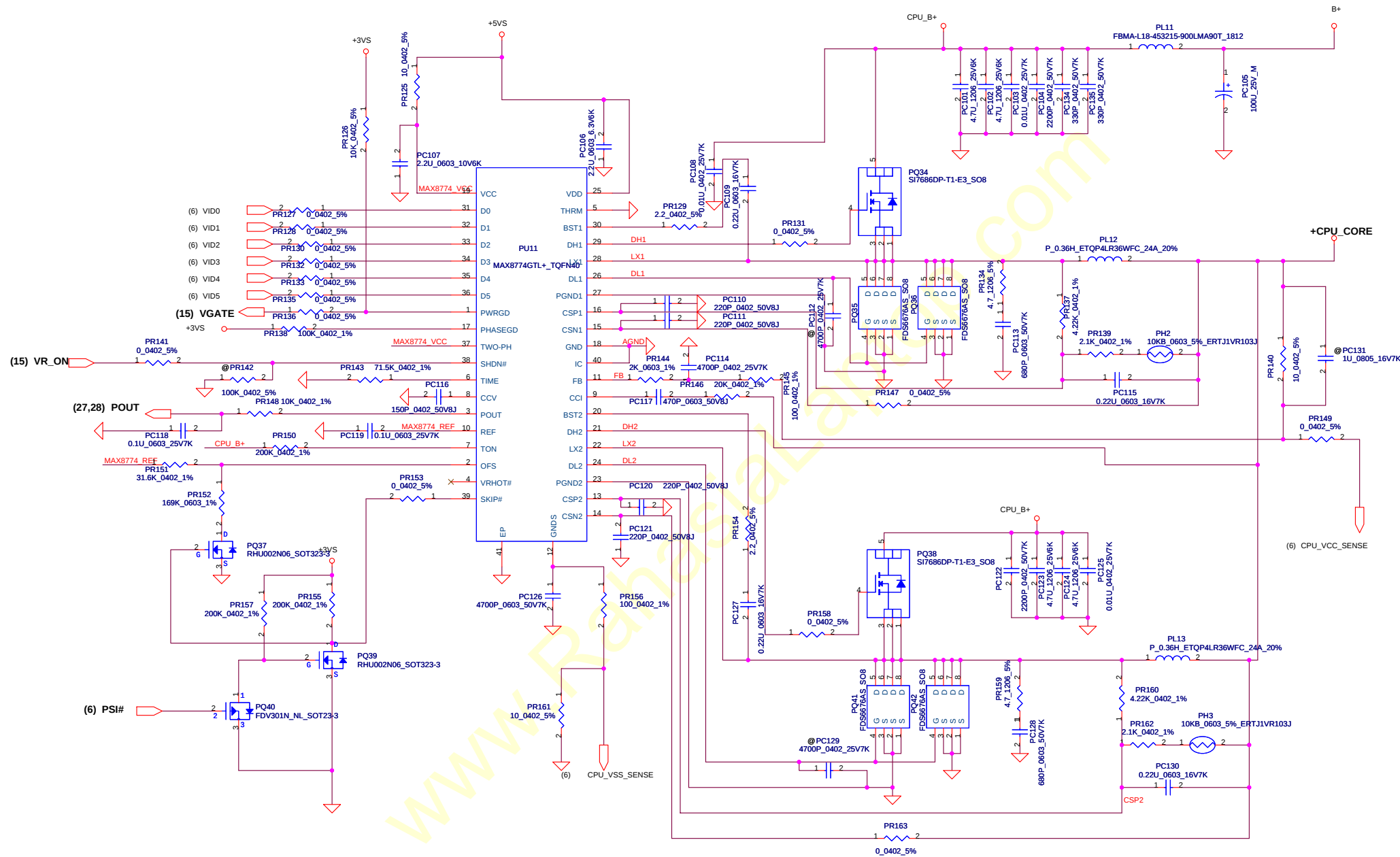
BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

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Deciphered Date				2007/09/01				CHARGER			
Size				Document Number				Rev			
Date				Friday, April 20, 2007				Sheet			
38				42				1.0			

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						Size	Document Number		Rev		
							ICW50 / ICY70		1.0		
						Date:	Friday, April 20, 2007		Sheet 39 of 42		
						3		1		2	



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Size	Custom	Document Number	ICW50/ICY70	Rev	
Date:		Friday, April 20, 2007		Sheet 41 of 42	

Item	Fixed Issue	Rev.	PG#	Modify List	Date	Phase
1	BOM Change.	0.4	12	Remove R144, R372, C160, C528.		PVT
2	Added SSC for Lan TXCLK. (EMI Request)	0.4	12	Added U40, R525, R526, R527, R528, C682.		PVT
3	Improve Samsung Memory Module compatibility.	0.4	15	Added R540,R541 2.2K pull up +3VS.		PVT
4	Design Modify. (SCH Change)	0.4	15	Change CRT_DET form GPIO_5 to LID#, Add R78 10K. (Bios Request)		PVT
5	BCIC0172 : When Reset or Cold Boot MCP67 ACIN 會漏電到EC.	0.4	15	D24 反向, 47K Pull High 移除. Added R283 200K Pull Down.		PVT
6	RTC Battery 電壓過低.	0.4	16	Added R539 1K.		PVT
7	Design Modify. (SCH Change)	0.4	22	Change Q50.G Pin Net Name to SBPWR_EN.		PVT
8	Added R-C for BUF_25Mhz (EMI Request).	0.4	22	Added R530,C684.		PVT
9	Design Modify for EMI.	0.4	22	Added L59, L60, L61, L62, C685, C686.		PVT
10	解決+3VS 漏電 when enter S3 Mode.	0.4	25,26	Added Q56, Q57, Q58, Q59, R536, R537.		PVT
11	Design Modify for Acer WLAN LED.	0.4	25	JP21.44 Pin Added MINI1_LED# Net, Added R520, R521.		PVT
12	防止 BATT_TEMP, BATT_OVP, ACIN 被干擾.	0.4	27	Added C660, C661, C662.		PVT
13	Design Modify for Power. (65W/95W Detect Function)	0.4	27	U15.98 Pin Added 65W/95W# Net, Added R519 100K to +3VALW.		PVT
14	Design Modify for EMI.	0.4	30	Added C663~C678.		PVT
15	For AUDIO EA Test.	0.4	32	Change C582, C583, C584, C587,C594, C597 to 4.7uF.		PVT
16	解決關機 bo bo 聲問題.	0.4	33	Added Q53,C680.		PVT
17	Design Modify for EMI.	0.4	33	Added L57, L58 for Mic. L63, L64, L65, L66 for SPK. D28 for ESD.		PVT
18	Change Codec Amp to APA2057RI-TRL_TSSOP28.	0.4	33	Change U31 to SA00001QD00, added R523,R524.		PVT
19	Remove PJP14.	0.4	34	Remove PJP14.		PVT
20	Change MCP67-MV form A01 to A02.	0.4	10~17	Change MCP67-MV form A01 to A02.		PVT
21	解決系統時間延遲問題.	0.4	15	Change C503, C504 form 18pF to 6.8pF.		PVT
22	Improve WLAN Module compatibility.	0.3	11,25	Change WLAN Port form PCIE4 to PCIE2.		DVT2
23	Fixed LAN LED work abnormal.	0.3	22	Added D25,D27,D27, U39.		DVT2
24	Change LAN to RTL8211B.	0.2	22	Change Page 22 all compnent.	DVT1	